VIPA System 200V

CPU | Manual

HB97E_CPU | RE_21x-2BS03 | Rev. 15/16

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VIPA

A YASKAWA COMPANY

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VIPA, Gesellschaft für Visualisierung und Prozessautomatisierung mbH
Ohmstraße 4, D-91074 Herzogenaurach, Germany
Tel.: +49 (91 32) 744 -0
Fax.: +49 9132 744 1864
EMail: info@vipa.de
http://www.vipa.com

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VIPA GmbH, Ohmstraße 4, 91074 Herzogenaurach, Germany

Telefax:+49 9132 744 1204
EMail: documentation@vipa.de

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Contact your local VIPA Customer Service Organization representative if you encounter problems with the product or have questions regarding the product. If you are unable to locate a customer service center, contact VIPA as follows:

VIPA GmbH, Ohmstraße 4, 91074 Herzogenaurach, Germany

Telephone: +49 9132 744 1150 (Hotline)
EMail: support@vipa.de

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About this manual

This manual describes the System 200V CPU 21x-2BS03 from VIPA. Here you may find every information for commissioning and operation.

Overview

Chapter 1: Basics and Assembly

The focus of this chapter is on the introduction of the VIPA System 200V. Here you will find the information required to assemble and wire a controller system consisting of System 200V components.
Besides the dimensions the general technical data of System 200V will be found.

Chapter 2: Hardware description

Here the hardware components of the CPU are described. The technical data are at the end of the chapter.

Chapter 3: Deployment CPU 21x-2BS03

This chapter describes the deployment of the CPU in the System 200V. The description refers directly to the CPU and to the deployment in connection with peripheral modules, mounted on a profile rail together with the CPU at the backplane bus.

Chapter 4: Serial communication

Content of this chapter is the usage of the two serial RS232 interfaces of the CPU. Here you'll find all information about the deployment of the serial interfaces of the CPU.

Objective and contents

This manual describes the System 200V CPU 21x-2BS03 from VIPA.
It contains a description of the construction, project implementation and usage.

This manual is part of the documentation package with order number HB97E_CPU and relevant for:

Product	Order number	as of state:	
		CPU-HW	CPU-FW
CPU 21xSER	VIPA CPU 21x-2BS03	01	V 4.1.7

Target audience

The manual is targeted at users who have a background in automation technology.

Structure of the manual

The manual consists of chapters. Every chapter provides a self-contained description of a specific topic.

Guide to the document

The following guides are available in the manual:

- an overall table of contents at the beginning of the manual
- an overview of the topics for every chapter

Availability

The manual is available in:

- printed form, on paper
- in electronic form as PDF-file (Adobe Acrobat Reader)

Icons Headings

Important passages in the text are highlighted by following icons and headings:

Danger!
Immediate or likely danger.
Personal injury is possible.

Attention!
Damages to property is likely if these warnings are not heeded.

Note!
Supplementary information and useful tips.

Safety information

Applications conforming with specifications

The CPU 21x is constructed and produced for:

- all VIPA System 200V components
- communication and process control
- general control and automation applications
- industrial applications
- operation within the environmental conditions specified in the technical data
- installation into a cubicle

Danger!

This device is not certified for applications in

- in explosive environments (EX-zone)

Documentation

The manual must be available to all personnel in the

- project design department
- installation department
- commissioning
- operation

The following conditions must be met before using or commissioning the components described in this manual:

- Hardware modifications to the process control system should only be carried out when the system has been disconnected from power!
- Installation and hardware modification only by properly trained personnel.
- The national rules and regulations of the respective country must be satisfied (installation, safety, EMC ...)

Disposal

National rules and regulations apply to the disposal of the unit!

Chapter 1 Basics and Assembly

Overview

The focus of this chapter is on the introduction of the VIPA System 200V. Here you will find the information required to assemble and wire a controller system consisting of System 200V components.

Besides the dimensions the general technical data of System 200V will be found.

Contents

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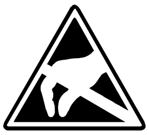
Safety Information for Users

Handling of electrostatic sensitive modules

VIPA modules make use of highly integrated components in MOS-Technology. These components are extremely sensitive to over-voltages that can occur during electrostatic discharges.

The following symbol is attached to modules that can be destroyed by electrostatic discharges.



The Symbol is located on the module, the module rack or on packing material and it indicates the presence of electrostatic sensitive equipment.

It is possible that electrostatic sensitive equipment is destroyed by energies and voltages that are far less than the human threshold of perception. These voltages can occur where persons do not discharge themselves before handling electrostatic sensitive modules and they can damage components thereby, causing the module to become inoperable or unusable.

Modules that have been damaged by electrostatic discharges can fail after a temperature change, mechanical shock or changes in the electrical load.

Only the consequent implementation of protection devices and meticulous attention to the applicable rules and regulations for handling the respective equipment can prevent failures of electrostatic sensitive modules.

Shipping of electrostatic sensitive modules

Modules must be shipped in the original packing material.

Measurements and alterations on electrostatic sensitive modules

When you are conducting measurements on electrostatic sensitive modules you should take the following precautions:

- Floating instruments must be discharged before use.
- Instruments must be grounded.

Modifying electrostatic sensitive modules you should only use soldering irons with grounded tips.

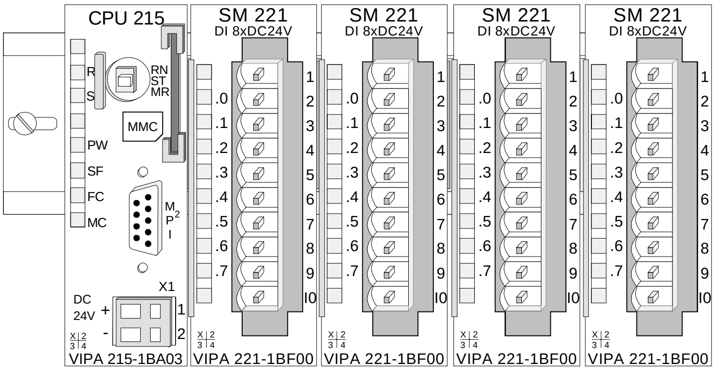
Attention!

Personnel and instruments should be grounded when working on electrostatic sensitive modules.

System conception

Overview

The System 200V is a modular automation system for assembly on a 35mm profile rail. By means of the peripheral modules with 4, 8 and 16 channels this system may properly be adapted matching to your automation tasks.

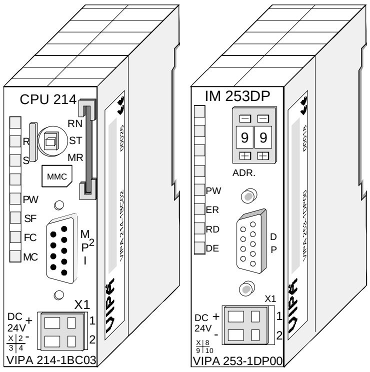


Components

The System 200V consists of the following components:

- *Head modules* like CPU and bus coupler
- *Periphery modules* like I/O, function und communication modules
- *Power supplies*
- *Extension modules*

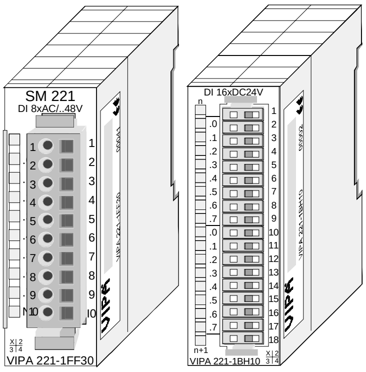
Head modules



With a head module CPU respectively bus interface and DC 24V power supply are integrated to one casing.

Via the integrated power supply the CPU respectively bus interface is power supplied as well as the electronic of the connected periphery modules.

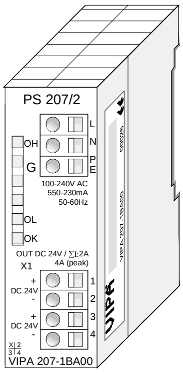
Periphery modules



The modules are direct installed on a 35mm profile rail and connected to the head module by a bus connector, which was mounted on the profile rail before.

Most of the periphery modules are equipped with a 10pin respectively 18pin connector. This connector provides the electrical interface for the signaling and supplies lines of the modules.

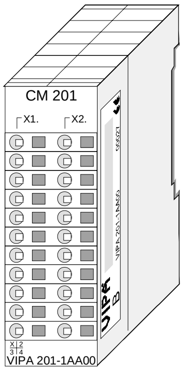
Power supplies



With the System 200V the DC 24V power supply can take place either externally or via a particularly for this developed power supply.

The power supply may be mounted on the profile rail together with the System 200V modules. It has no connector to the backplane bus.

Expansion modules



The expansion modules are complementary modules providing 2- or 3wire connection facilities.

The modules are not connected to the backplane bus.

Structure/ dimensions

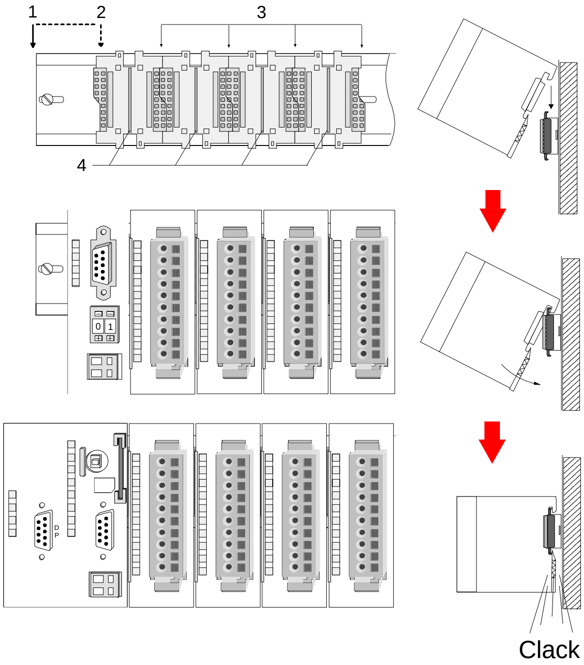
- Profile rail 35mm
- Dimensions of the basic enclosure:

  1tier width: (HxWxD) in mm: 76x25.4x74 in inches: 3x1x3

  2tier width: (HxWxD) in mm: 76x50.8x74 in inches: 3x2x3

Installation

Please note that you can only install header modules, like the CPU, the PC and couplers at slot 1 or 1 and 2 (for double width modules).



[1]	Head module (double width)
[2]	Head module (single width)
[3]	Periphery module
[4]	Guide rails

Note

A maximum of 32 modules can be connected at the back plane bus. Take attention that here the **maximum sum current** of **3.5A** is not exceeded.

Please install modules with a high current consumption directly beside the header module.

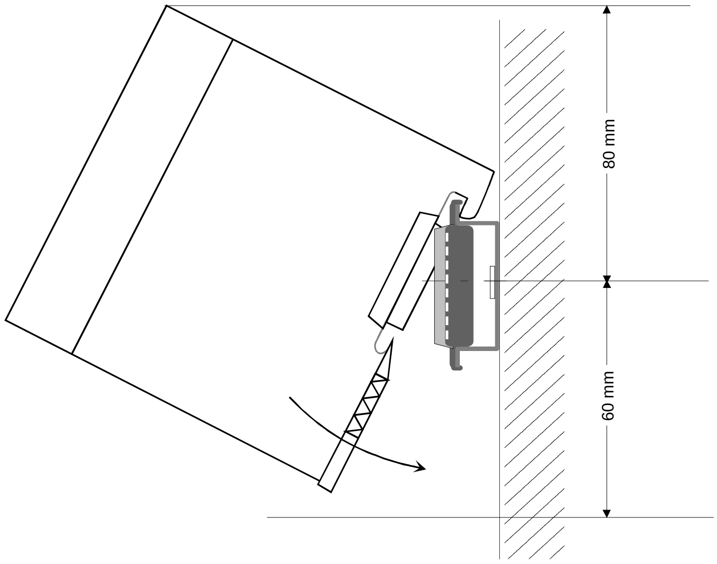
Dimensions

Dimensions Basic enclosure

1tier width (HxWxD) in mm: 76 x 25.4 x 74

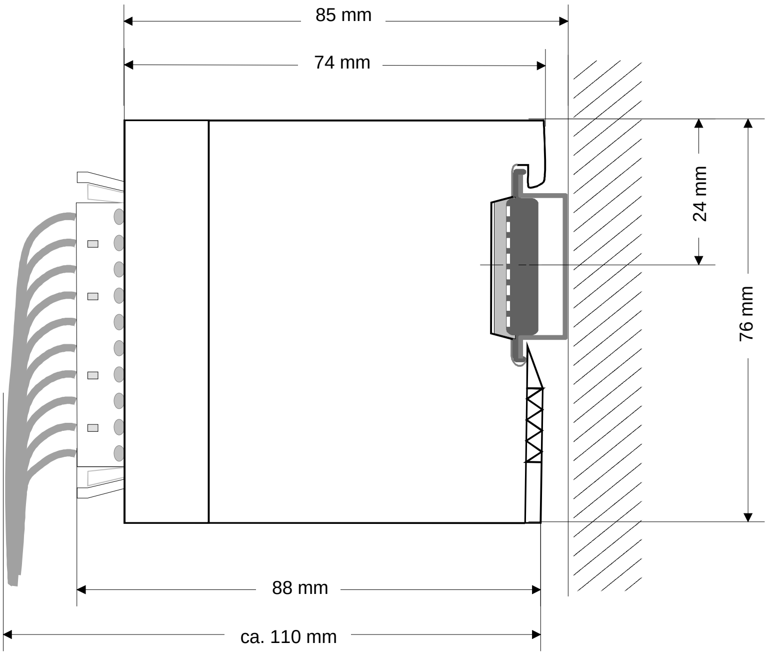
2tier width (HxWxD) in mm: 76 x 50.8 x 74

Installation dimensions

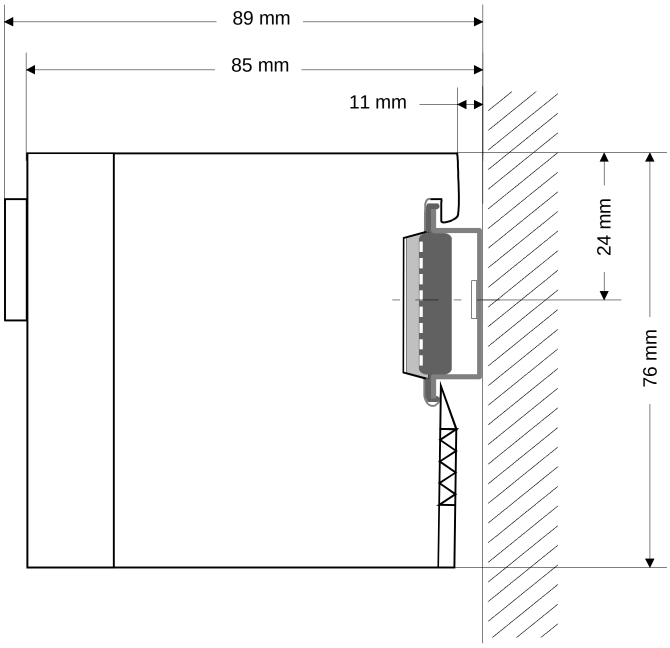


Installed and wired dimensions

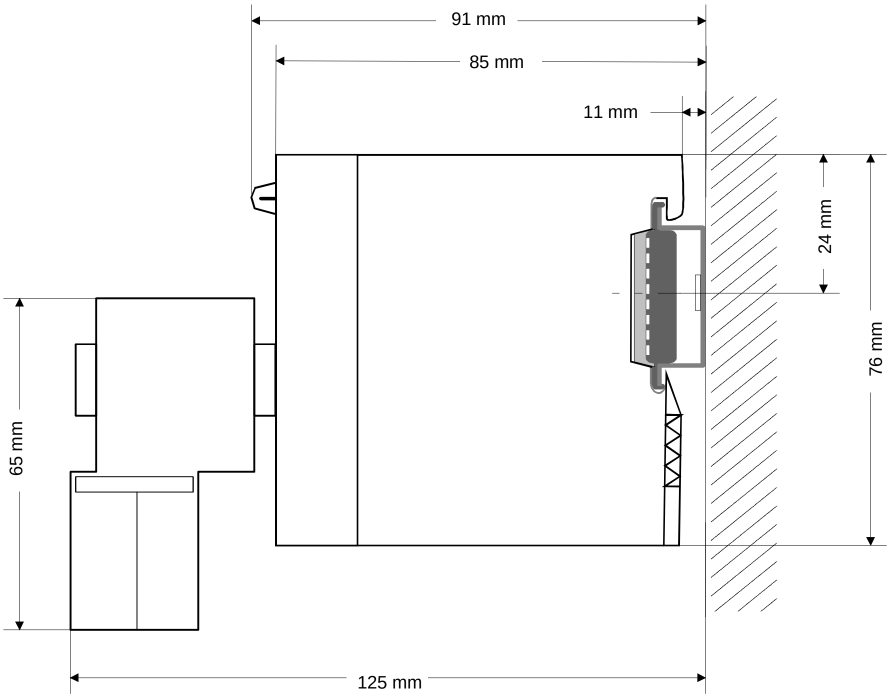
In- / Output modules



Function modules/
Extension modules



CPUs (here with
EasyConn from
VIPA)



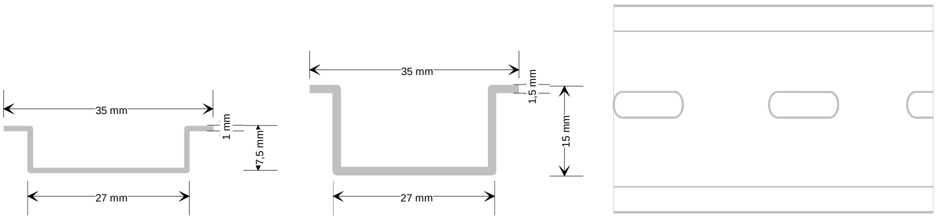
Installation

General

The modules are each installed on a 35mm profile rail and connected via a bus connector. Before installing the module the bus connector is to be placed on the profile rail before.

Profile rail

For installation the following 35mm profile rails may be used:

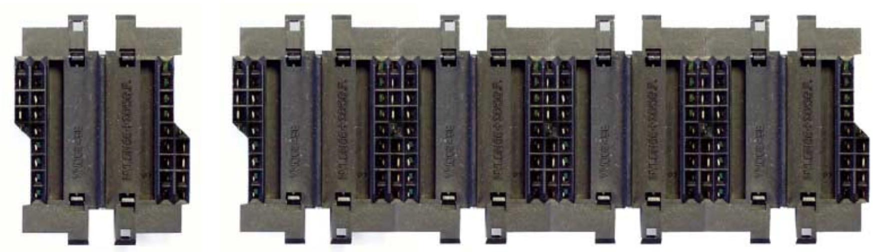


Order number	Label	Description
290-1AF00	35mm profile rail	Length 2000mm, height 15mm
290-1AF30	35mm profile rail	Length 530mm, height 15mm

Bus connector

System 200V modules communicate via a backplane bus connector. The backplane bus connector is isolated and available from VIPA in of 1-, 2-, 4- or 8tier width.

The following figure shows a 1tier connector and a 4tier connector bus:



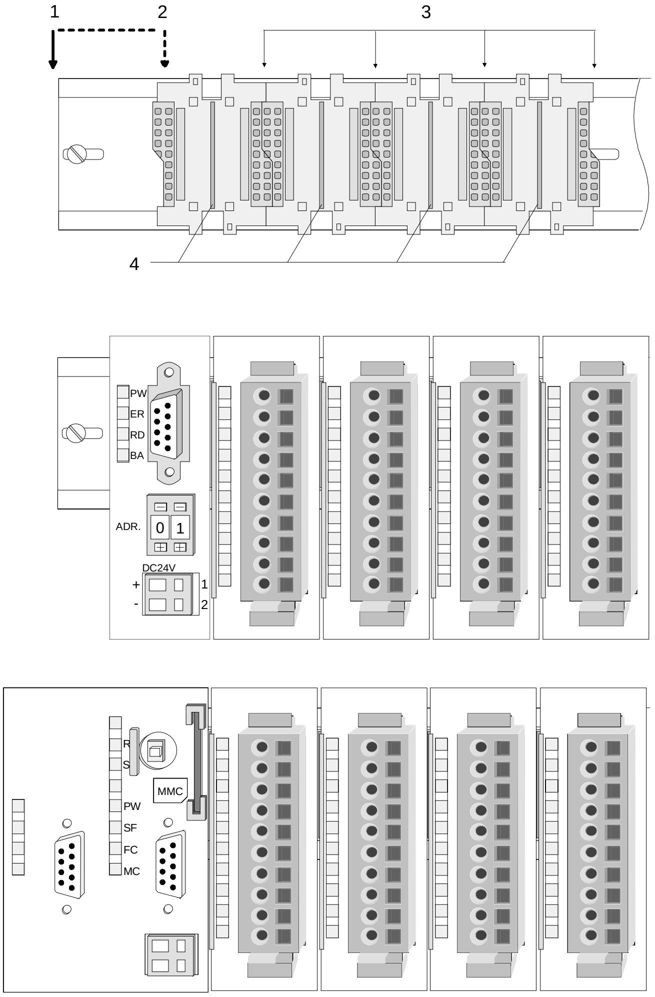
The bus connector is to be placed on the profile rail until it clips in its place and the bus connections look out from the profile rail.

Order number	Label	Description
290-0AA10	Bus connector	1tier
290-0AA20	Bus connector	2tier
290-0AA40	Bus connector	4tier
290-0AA80	Bus connector	8tier

Installation on a profile rail

The following figure shows the installation of a 4tier width bus connector in a profile rail and the slots for the modules.

The different slots are defined by guide rails.

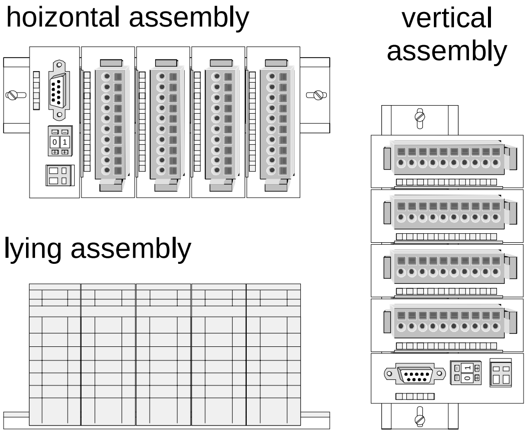


[1] Header module (double width)
[2] Header module (single width)
[3] Peripheral module
[4] Guide rails

Assembly regarding the current consumption

- Use bus connectors as long as possible.
- Sort the modules with a high current consumption right beside the header module. In the service area of www.vipa.com a list of current consumption of every System 200V module can be found.

Assembly possibilities

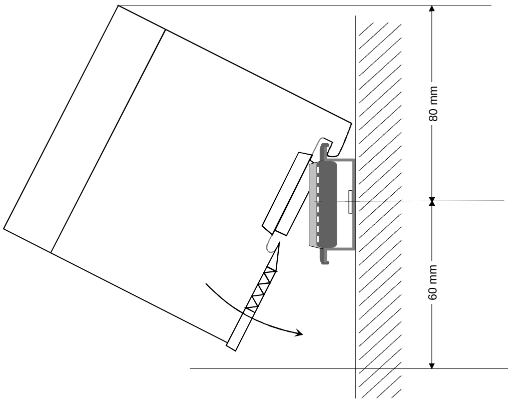


Please regard the allowed environmental temperatures:

- horizontal assembly: from 0 to 60°C
- vertical assembly: from 0 to 40°C
- lying assembly: from 0 to 40°C

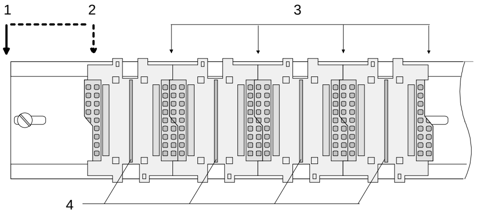
The horizontal assembly always starts at the left side with a header module, then you install the peripheral modules beside to the right.

You may install up to 32 peripheral modules.



Please follow these rules during the assembly!

- Turn off the power supply before you install or remove any modules!
- Make sure that a clearance of at least 60mm exists above and 80mm below the middle of the profile rail.



- Every row must be completed from left to right and it has to start with a header module.

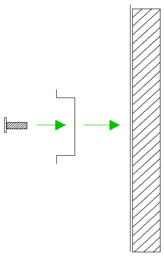
[1] Header module (double width)
[2] Header module (single width)
[3] Peripheral modules
[4] Guide rails

- Modules are to be installed side by side. Gaps are not permitted between the modules since this would interrupt the backplane bus.
- A module is only installed properly and connected electrically when it has clicked into place with an audible click.
- Slots after the last module may remain unoccupied.

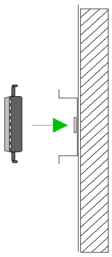
Note!

A maximum of 32 modules can be connected at the back plane bus. Take attention that here the maximum **sum current** of **3.5A** is not exceeded.

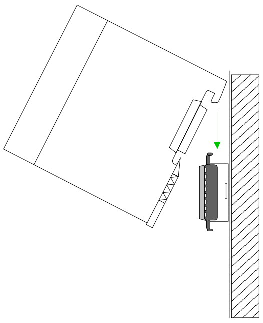
Assembly procedure



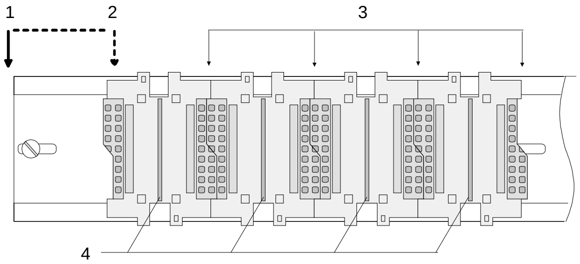
- Install the profile rail. Make sure that a clearance of at least 60mm exists above and 80mm below the middle of the profile rail.



- Press the bus connector into the profile rail until it clips securely into place and the bus-connectors look out from the profile rail. This provides the basis for the installation of your modules.



- Start at the outer left location with the installation of your header module and install the peripheral modules to the right of this.

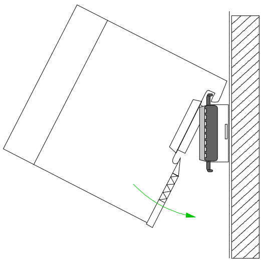


[1] Header module (double width)

[2] Header module (single width)

[3] Peripheral module

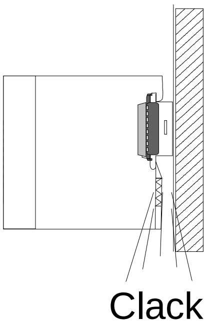
[4] Guide rails



- Insert the module that you are installing into the profile rail at an angle of 45 degrees from the top and rotate the module into place until it clicks into the profile rail with an audible click. The proper connection to the backplane bus can only be guaranteed when the module has properly clicked into place.

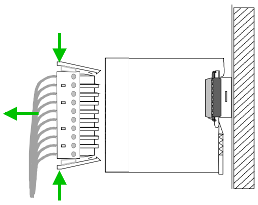
Attention!

Power must be turned off before modules are installed or removed!



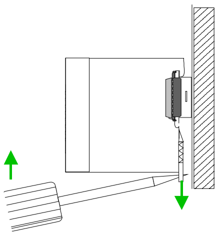
Demounting and module exchange

1



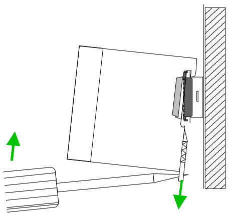
- Remove if exists the wiring to the module, by pressing both locking lever on the connector and pulling the connector.

2



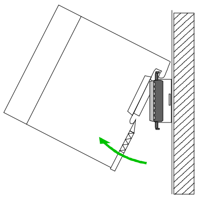
- The casing of the module has a spring loaded clip at the bottom by which the module can be removed.

3



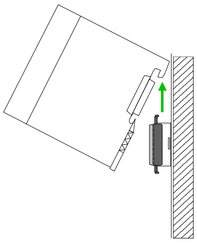
- The clip is unlocked by pressing the screwdriver in an upward direction.

4



- Withdraw the module with a slight rotation to the top.

5



Attention!

Power must be turned off before modules are installed or removed!

Please regard that the backplane bus is interrupted at the point where the module was removed!

Wiring

Overview

Most peripheral modules are equipped with a 10pole or a 18pole connector. This connector provides the electrical interface for the signaling and supply lines of the modules.

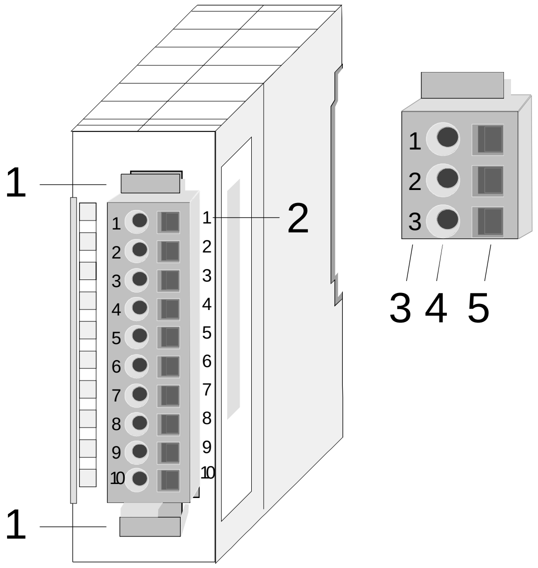
The modules carry spring-clip connectors for interconnections and wiring.

The spring-clip connector technology simplifies the wiring requirements for signaling and power cables.

In contrast to screw terminal connections, spring-clip wiring is vibration proof. The assignment of the terminals is contained in the description of the respective modules.

You may connect conductors with a diameter from 0.08mm^2 up to 2.5mm^2 (max. 1.5mm^2 for 18pole connectors).

The following figure shows a module with a 10pole connector.



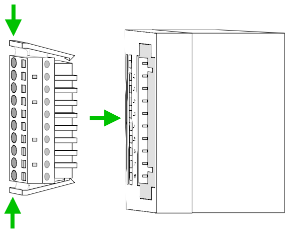
[1] Locking lever
[2] Pin no. at the module
[3] Pin no. at the connector
[4] Wiring port
[5] Opening for screwdriver

Note!

The spring-clip is destroyed if you push the screwdriver into the wire port!

Make sure that you only insert the screwdriver into the square hole of the connector!

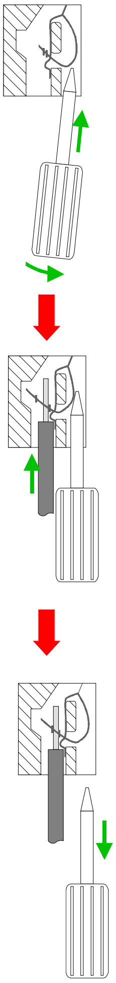
Wiring procedure



- Install the connector on the module until it locks with an audible click. For this purpose you press the two clips together as shown.

  The connector is now in a permanent position and can easily be wired.

The following section shows the wiring procedure from top view.



- Insert a screwdriver at an angel into the square opening as shown.
- Press and hold the screwdriver in the opposite direction to open the contact spring.

- Insert the stripped end of the wire into the round opening. You can use wires with a diameter of 0.08mm^2 to 2.5mm^2 (1.5mm^2 for 18pole connectors).

- By removing the screwdriver the wire is connected safely with the plug connector via a spring.

Note!

Wire the power supply connections first followed by the signal cables (inputs and outputs).

Installation guidelines

General

The installation guidelines contain information about the interference free deployment of System 200V systems. There is the description of the ways, interference may occur in your control, how you can make sure the electromagnetic digestibility (EMC), and how you manage the isolation.

What means EMC?

Electromagnetic digestibility (EMC) means the ability of an electrical device, to function error free in an electromagnetic environment without being interferenced res. without interferencing the environment.

All System 200V components are developed for the deployment in hard industrial environments and fulfill high demands on the EMC. Nevertheless you should project an EMC planning before installing the components and take conceivable interference causes into account.

Possible interference causes

Electromagnetic interferences may interfere your control via different ways:

- Electromagnetic fields (RF coupling)
- Magnetic fields with power frequency
- I/O signal conductors
- Bus system
- Current supply
- Protected earth conductor

Depending on the spreading medium (lead bound or lead free) and the distance to the interference cause, interferences to your control occur by means of different coupling mechanisms.

One differs:

- galvanic coupling
- capacitive coupling
- inductive coupling
- radiant coupling

Basic rules for EMC

In the most times it is enough to take care of some elementary rules to guarantee the EMC. Please regard the following basic rules when installing your PLC.

- Take care of a correct area-wide grounding of the inactive metal parts when installing your components.
  - Install a central connection between the ground and the protected earth conductor system.
  - Connect all inactive metal extensive and impedance-low.
  - Please try not to use aluminum parts. Aluminum is easily oxidizing and is therefore less suitable for grounding.
- When cabling, take care of the correct line routing.
  - Organize your cabling in line groups (high voltage, current supply, signal and data lines).
  - Always lay your high voltage lines and signal res. data lines in separate channels or bundles.
  - Route the signal and data lines as near as possible beside ground areas (e.g. suspension bars, metal rails, tin cabinet).
- Proof the correct fixing of the lead isolation.
  - Data lines must be laid isolated (for details see below).
  - Analog lines must be laid isolated. When transmitting signals with small amplitudes the one sided laying of the isolation may be favorable.
  - Lay the line isolation extensively on an isolation/protected earth conductor rail directly after the cabinet entry and fix the isolation with cable clamps.
  - Make sure that the isolation/protected earth conductor rail is connected impedance-low with the cabinet.
  - Use metallic or metalized plug cases for isolated data lines.
- In special use cases you should appoint special EMC actions.
  - Wire all inductivities with erase links, which are not addressed by the System SLIO modules.
  - For lightening cabinets you should avoid luminescent lamps.
- Create a homogeneous reference potential and ground all electrical operating supplies when possible.
  - Please take care for the targeted employment of the grounding actions. The grounding of the PLC is a protection and functionality activity.
  - Connect installation parts and cabinets with the System SLIO in star topology with the isolation/protected earth conductor system. So you avoid ground loops.
  - If potential differences between installation parts and cabinets occur, lay sufficiently dimensioned potential compensation lines.

Isolation of conductors

Electrical, magnetically and electromagnetic interference fields are weakened by means of an isolation, one talks of absorption.

Via the isolation rail, that is connected conductive with the rack, interference currents are shunt via cable isolation to the ground. Hereby you have to make sure, that the connection to the protected earth conductor is impedance-low, because otherwise the interference currents may appear as interference cause.

When isolating cables you have to regard the following:

- If possible, use only cables with isolation tangle.
- The hiding power of the isolation should be higher than 80%.
- Normally you should always lay the isolation of cables on both sides. Only by means of the both-sided connection of the isolation you achieve high quality interference suppression in the higher frequency area.

  Only as exception you may also lay the isolation one-sided. Then you only achieve the absorption of the lower frequencies. A one-sided isolation connection may be convenient, if:

  - the conduction of a potential compensating line is not possible
  - analog signals (some mV res. µA) are transferred
  - foil isolations (static isolations) are used.
- With data lines always use metallic or metalized plugs for serial couplings. Fix the isolation of the data line at the plug rack. Do not lay the isolation on the PIN 1 of the plug bar!
- At stationary operation it is convenient to strip the insulated cable interruption free and lay it on the isolation/protected earth conductor line.
- To fix the isolation tangles use cable clamps out of metal. The clamps must clasp the isolation extensively and have well contact.
- Lay the isolation on an isolation rail directly after the entry of the cable in the cabinet. Lead the isolation further on to the System 200V module and **don't** lay it on there again!

Please regard at installation!

At potential differences between the grounding points, there may be a compensation current via the isolation connected at both sides.

Remedy: Potential compensation line.

General data

Structure/ dimensions

- Profile rail 35mm
- Peripheral modules with recessed labelling
- Dimensions of the basic enclosure:
  1tier width: (HxWxD) in mm: 76x25.4x74 in inches: 3x1x3
  2tier width: (HxWxD) in mm: 76x50.8x74 in inches: 3x2x3

Reliability

- Wiring by means of spring pressure connections (CageClamps) at the front-facing connector, core cross-section 0.08 ... 2.5mm^2 or 1.5mm^2 (18pole plug)
- Complete isolation of the wiring when modules are exchanged
- Every module is isolated from the backplane bus

General data

Conformity and approval		
Conformity		
CE	2006/95/EC	Low-voltage directive
	2004/108/EC	EMC directive
Approval		
UL	UL 508	Approval for USA and Canada
others		
RoHS	2011/65/EU	Product is lead-free; Restriction of the use of certain hazardous substances in electrical and electronic equipment

Protection of persons and device protection		
Type of protection	-	IP20
Electrical isolation		
to the field bus	-	electrically isolated
to the process level	-	electrically isolated
Insulation resistance	EN 61131-2	-
Insulation voltage to reference earth		
Inputs / outputs	-	AC / DC 50V, test voltage AC 500V
Protective measures	-	against short circuit

Environmental conditions to EN 61131-2		
Climatic		
Storage / transport	EN 60068-2-14	-25…+70°C
Operation		
Horizontal installation	EN 61131-2	0…+60°C
Vertical installation	EN 61131-2	0…+60°C
Air humidity	EN 60068-2-30	RH1 (without condensation, rel. humidity 10…95%)
Pollution	EN 61131-2	Degree of pollution 2
Mechanical		
Oscillation	EN 60068-2-6	1g, 9Hz ... 150Hz
Shock	EN 60068-2-27	15g, 11ms

Mounting conditions		
Mounting place	-	In the control cabinet
Mounting position	-	Horizontal and vertical

EMC	Standard		Comment
Emitted interference	EN 61000-6-4		Class A (Industrial area)
Noise immunity zone B	EN 61000-6-2		Industrial area
		EN 61000-4-2	ESD 8kV at air discharge (degree of severity 3), 4kV at contact discharge (degree of severity 2)
		EN 61000-4-3	HF field immunity (casing) 80MHz … 1000MHz, 10V/m, 80% AM (1kHz) 1.4GHz ... 2.0GHz, 3V/m, 80% AM (1kHz) 2GHz ... 2.7GHz, 1V/m, 80% AM (1kHz)
		EN 61000-4-6	HF conducted 150kHz … 80MHz, 10V, 80% AM (1kHz)
		EN 61000-4-4	Burst, degree of severity 3
		EN 61000-4-5	Surge, installation class 3 *)

*) Due to the high-energetic single pulses with Surge an appropriate external protective circuit with lightning protection elements like conductors for lightning and overvoltage is necessary.

Chapter 2 Hardware description

Overview

Here the hardware components of the CPU are described. The technical data are at the end of the chapter.

Contents

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Properties.. 2-2
Structure 2-3
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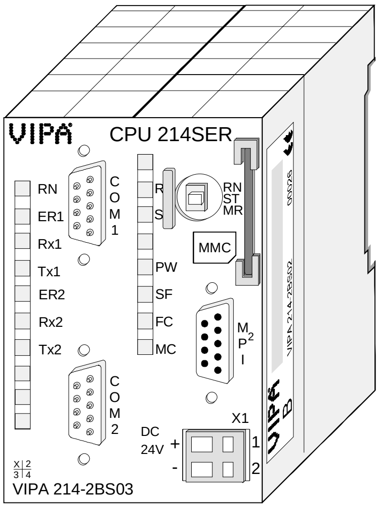
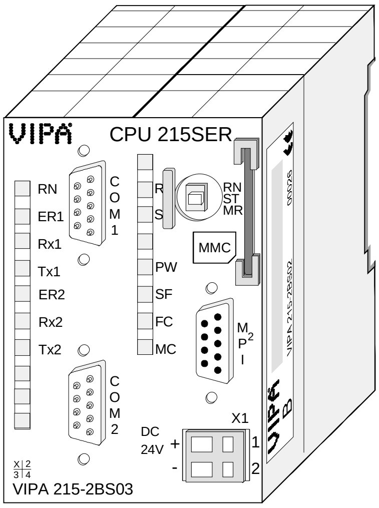
Properties

CPU 21x-2BS03

- Instruction set compatible with Siemens STEP®7
- Configuration by means of the Siemens SIMATIC manager
- Integrated V-Bus controller for controlling System 200V peripherals
- Integrated 24V power supply
- Total address range: 1024Byte inputs, 1024Byte outputs (128Byte process image each)
- 96 / 128kByte of work memory "on board"
- 144 / 192kByte of load memory "on board"
- MMC slot (for user program)
- Battery backed clock
- MP^{2}I interface for data transfer
- Status LEDs for operating mode and diagnostics
- Serial Communication via 2x RS232 interface



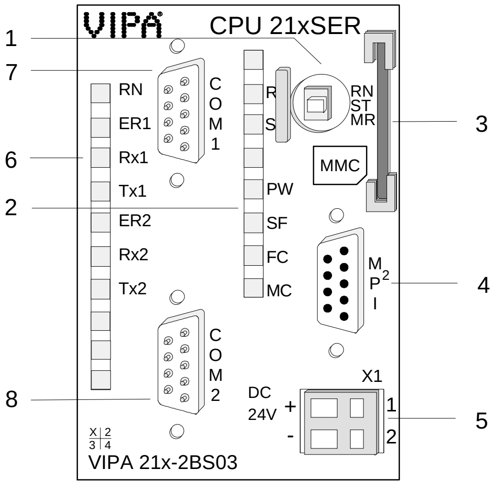


Order data

Type	Order number	Description
CPU 214SER	VIPA 214-2BS03	PLC CPU 214 with 2xRS322 interface 96/144kByte of work/load memory
CPU 215SER	VIPA 215-2BS03	PLC CPU 215 with 2xRS322 interface 128/192kByte of work/load memory

Structure

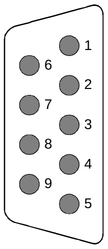
Front view CPU 21xSER



[1] Operating mode switch
[2] LEDs of the CPU
[3] Slot for MMC memory card
[4] MP^2I interface
[5] Slot for DC 24V power supply
[6] LED of the RS232 interfaces
[7] RS232 interface COM1
[8] RS232 interface COM2

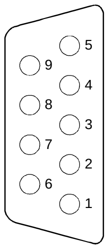
Interfaces

COM1
RS232



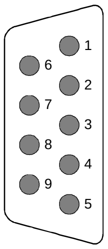
①	CD-
②	RxD
③	TxD
④	DTR-
⑤	GND
⑥	DSR-
⑦	RTS-
⑧	CTS-
⑨	RI-

MP^2I



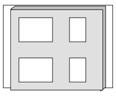
①	reserved
②	M24V
③	RxD/TxD-P (line B)
④	RTS
⑤	M5V
⑥	P5V
⑦	P24V
⑧	RxD/TxD-N (line A)
⑨	n.c.

COM2
RS232



①	CD-
②	RxD
③	TxD
④	DTR-
⑤	GND
⑥	DSR-
⑦	RTS-
⑧	CTS-
⑨	RI-

X1



+	①	+ DC 24 V
-	②	0 V

Power supply

The CPU has an internal power supply. This is connected to an external supply voltage via two terminals located on the front of the unit.

The power supply requires DC 24V (20.4 ... 28.8V). In addition to the electronic circuitry of the CPU this supply voltage is used for the modules connected to the backplane bus.

The electronic circuitry of the CPU is not dc-insulated from the supply voltage. The power supply is protected against reverse polarity and short circuits.

Note!

Please ensure that the polarity of the supply voltage is correct.

MP^{2}I interface

The MPI unit provides the link for the data transfer between the CPU and the PC. Via bus communication you are able to exchange programs and data between different CPUs that are linked over MPI.

For a serial exchange between the partners you normally need a special MPI-converter. But now you are also able to use the VIPA "Green Cable" (Order-No. VIPA 950-0KB00), which allows you to establish a serial peer-to-peer connection over the MPI interface.

Please regard the "Hints for the deployment of the MPI interface" in chapter "Deployment CPU 21x".

RS232 interface COM1, COM2

Additional to the components described before, the CPU has two RS232 interfaces.

Via the 9pin interface you may establish serial RS232 point-to-point connections.

Note!

More information about the serial communication may be found in the chapter "Serial communication".

Memory management

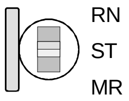
The CPUs have an integrated work and a load memory. The memories are battery-buffered.

Order number	Work memory	Load memory
VIPA 214-2BS03	96kByte	144kByte
VIPA 215-2BS03	128kByte	192kByte

In the load memory there are program code and blocks stored together with the header information.

The program parts and blocks, which are relevant for the running program, are loaded to the work memory during the program sequence.

Operating mode switch



With the operating mode switch you may switch the CPU between STOP and RUN.
During the transition from STOP to RUN the operating mode START-UP is driven by the CPU.

By Switching to MR (Memory Reset) you request an overall reset with following load from MMC, if a project there exists.

MMC slot memory card

You may install a VIPA MMC memory card in this slot as external storage device (Order No.: VIPA 953-0KX10).

The access to the MMC takes always place after an overall reset.

Battery backup for clock and RAM

A rechargeable battery is installed on every CPU 21x to safeguard the contents of the RAM when power is removed. This battery is also used to buffer the internal clock.

The rechargeable battery is maintained by a charging circuit that receives its power from the internal power supply and that maintain the clock and RAM for a max. period of 30 days.

Attention!

Due to a long storage of the CPU, the battery may be discharged excessively. Please connect the CPU at least for 24 hours to the power supply, to achieve the full buffer capacity.

After a power reset and with an empty battery the CPU starts with a BAT error and executes an overall reset, because with an empty battery the RAM content is undefined.

LEDs CPU

The CPU has got LEDs on its front side. In the following the usage and the according colors of the LEDs is described.

Name	Color	Description
PW	green	Indicates CPU power on.
R	green	CPU status is RUN.
S	yellow	CPU status is STOP.
SF	red	Is turned on if a system error is detected (hardware defect)
FC	yellow	Is turned on when variables are forced (fixed).
MC	yellow	This LED blinks when the MMC is accessed.

LEDs RS232

The LEDs of the RS232 interfaces are located in the left half of the front panel and they are used for diagnostic purposes. The following table shows the color and the significance of these LEDs.

Name	Color	Description
RN	green	Communication processor runs
ER1	red	Error Interface 1
Rx1	green	Interface 1 receive data
Tx1	green	Interface 1 transmit data
ER2	red	Error Interface 2
Rx2	green	Interface 2 receive data
Tx2	green	Interface 2 transmit data

Technical data

214-2BS03

Order no.	**214-2BS03**
Type	CPU 214SER
Technical data power supply	
Power supply (rated value)	DC 24 V
Power supply (permitted range)	DC 20.4...28.8 V
Reverse polarity protection	✓
Current consumption (no-load operation)	90 mA
Current consumption (rated value)	1.5 A
Inrush current	65 A
I^2t	0.75 A^2s
Max. current drain at backplane bus	3 A
Power loss	5 W
Load and working memory	
Load memory, integrated	144 KB
Load memory, maximum	144 KB
Work memory, integrated	96 KB
Work memory, maximal	96 KB
Memory divided in 50% program / 50% data	-
Memory card slot	MMC-Card with max. 512 MB
Hardware configuration	
Racks, max.	4
Modules per rack, max.	total max. 32
Number of integrated DP master	-
Number of DP master via CP	8
Operable function modules	32
Operable communication modules PtP	32
Operable communication modules LAN	-
Command processing times	
Bit instructions, min.	0.18 µs
Word instruction, min.	0.78 µs
Double integer arithmetic, min.	1.8 µs
Floating-point arithmetic, min.	40 µs
Timers/Counters and their retentive characteristics	
Number of S7 counters	256
S7 counter remanence	adjustable 0 up to 64
S7 counter remanence adjustable	C0 .. C7
Number of S7 times	256
S7 times remanence	adjustable 0 up to 128
S7 times remanence adjustable	not retentive
Data range and retentive characteristic	
Number of flags	8192 Bit
Bit memories retentive characteristic adjustable	adjustable 0 up to 256
Bit memories retentive characteristic preset	MB0 .. MB15
Number of data blocks	2047
Max. data blocks size	16 KB
Number range DBs	1 ... 2047
Max. local data size per execution level	1024 Byte
Max. local data size per block	1024 Byte
Blocks	
Number of OBs	14
Maximum OB size	16 KB
Total number DBs, FBs, FCs	-
Number of FBs	1024
Maximum FB size	16 KB
Number range FBs	0 ... 1023

Order no.	**214-2BS03**
Number of FCs	1024
Maximum FC size	16 KB
Number range FCs	0 ... 1023
Maximum nesting depth per priority class	8
Maximum nesting depth additional within an error OB	1
Time	
Real-time clock buffered	✓
Clock buffered period (min.)	30 d
Type of buffering	Vanadium Rechargeable Lithium Batterie
Load time for 50% buffering period	20 h
Load time for 100% buffering period	48 h
Accuracy (max. deviation per day)	10 s
Number of operating hours counter	8
Clock synchronization	-
Synchronization via MPI	-
Synchronization via Ethernet (NTP)	-
Address areas (I/O)	
Input I/O address area	1024 Byte
Output I/O address area	1024 Byte
Process image adjustable	-
Input process image preset	128 Byte
Output process image preset	128 Byte
Input process image maximal	128 Byte
Output process image maximal	128 Byte
Digital inputs	8192
Digital outputs	8192
Digital inputs central	512
Digital outputs central	512
Integrated digital inputs	-
Integrated digital outputs	-
Analog inputs	512
Analog outputs	512
Analog inputs, central	128
Analog outputs, central	128
Integrated analog inputs	-
Integrated analog outputs	-
Communication functions	
PG/OP channel	✓
Global data communication	✓
Number of GD circuits, max.	4
Size of GD packets, max.	22 Byte
S7 basic communication	✓
S7 basic communication, user data per job	76 Byte
S7 communication	✓
S7 communication as server	✓
S7 communication as client	-
S7 communication, user data per job	160 Byte
Number of connections, max.	16
Functionality Sub-D interfaces	
Type	MP²I
Type of interface	RS485
Connector	Sub-D, 9-pin, female
Electrically isolated	-
MPI	✓
MP²I (MPI/RS232)	✓
Point-to-point interface	-
Type	COM1
Type of interface	RS232

Order no.	**214-2BS03**
Connector	Sub-D, 9-pin, male
Electrically isolated	-
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	✓
Type	COM2
Type of interface	RS232
Connector	Sub-D, 9-pin, male
Electrically isolated	-
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	✓
Functionality MPI	
Number of connections, max.	16
PG/OP channel	✓
Routing	-
Global data communication	✓
S7 basic communication	✓
S7 communication	✓
S7 communication as server	✓
S7 communication as client	-
Transmission speed, min.	19.2 kbit/s
Transmission speed, max.	187.5 kbit/s
Point-to-point communication	
PtP communication	✓
Interface isolated	-
RS232 interface	✓
RS422 interface	-
RS485 interface	-
Connector	Sub-D, 9-pin, male
Transmission speed, min.	150 bit/s
Transmission speed, max.	115.2 kbit/s
Cable length, max.	15 m
Point-to-point protocol	
ASCII protocol	✓
STX/ETX protocol	✓
3964(R) protocol	✓
RK512 protocol	✓
USS master protocol	-
Modbus master protocol	-
Modbus slave protocol	-
Special protocols	-
Datasizes	
Input bytes	0
Output bytes	0
Parameter bytes	3
Diagnostic bytes	0
Housing	
Material	PPE / PA 6.6
Mounting	Profile rail 35 mm
Mechanical data	
Dimensions (WxHxD)	50.8 x 76 x 80 mm
Weight	150 g
Environmental conditions	
Operating temperature	0 °C to 60 °C
Storage temperature	-25 °C to 70 °C
Certifications	
UL508 certification	yes

215-2BS03

Order no.	**215-2BS03**
Type	CPU 215SER
Technical data power supply	
Power supply (rated value)	DC 24 V
Power supply (permitted range)	DC 20.4...28.8 V
Reverse polarity protection	✓
Current consumption (no-load operation)	90 mA
Current consumption (rated value)	1.5 A
Inrush current	65 A
I²t	0.75 A²s
Max. current drain at backplane bus	3 A
Power loss	5 W
Load and working memory	
Load memory, integrated	192 KB
Load memory, maximum	192 KB
Work memory, integrated	128 KB
Work memory, maximal	128 KB
Memory divided in 50% program / 50% data	-
Memory card slot	MMC-Card with max. 512 MB
Hardware configuration	
Racks, max.	4
Modules per rack, max.	total max. 32
Number of integrated DP master	-
Number of DP master via CP	8
Operable function modules	32
Operable communication modules PtP	32
Operable communication modules LAN	-
Command processing times	
Bit instructions, min.	0.18 µs
Word instruction, min.	0.78 µs
Double integer arithmetic, min.	1.8 µs
Floating-point arithmetic, min.	40 µs
Timers/Counters and their retentive characteristics	
Number of S7 counters	256
S7 counter remanence	adjustable 0 up to 64
S7 counter remanence adjustable	C0 .. C7
Number of S7 times	256
S7 times remanence	adjustable 0 up to 128
S7 times remanence adjustable	not retentive
Data range and retentive characteristic	
Number of flags	8192 Bit
Bit memories retentive characteristic adjustable	adjustable 0 up to 256
Bit memories retentive characteristic preset	MB0 .. MB15
Number of data blocks	2047
Max. data blocks size	16 KB
Number range DBs	1 ... 2047
Max. local data size per execution level	1024 Byte
Max. local data size per block	1024 Byte
Blocks	
Number of OBs	14
Maximum OB size	16 KB
Total number DBs, FBs, FCs	-
Number of FBs	1024
Maximum FB size	16 KB
Number range FBs	0 ... 1023
Number of FCs	1024
Maximum FC size	16 KB
Number range FCs	0 ... 1023
Maximum nesting depth per priority class	8
Maximum nesting depth additional within an error OB	1

Order no.	**215-2BS03**
Time	
Real-time clock buffered	✓
Clock buffered period (min.)	30 d
Type of buffering	Vanadium Rechargeable Lithium Batterie
Load time for 50% buffering period	20 h
Load time for 100% buffering period	48 h
Accuracy (max. deviation per day)	10 s
Number of operating hours counter	8
Clock synchronization	-
Synchronization via MPI	-
Synchronization via Ethernet (NTP)	-
Address areas (I/O)	
Input I/O address area	1024 Byte
Output I/O address area	1024 Byte
Process image adjustable	-
Input process image preset	128 Byte
Output process image preset	128 Byte
Input process image maximal	128 Byte
Output process image maximal	128 Byte
Digital inputs	8192
Digital outputs	8192
Digital inputs central	512
Digital outputs central	512
Integrated digital inputs	-
Integrated digital outputs	-
Analog inputs	512
Analog outputs	512
Analog inputs, central	128
Analog outputs, central	128
Integrated analog inputs	-
Integrated analog outputs	-
Communication functions	
PG/OP channel	✓
Global data communication	✓
Number of GD circuits, max.	4
Size of GD packets, max.	22 Byte
S7 basic communication	✓
S7 basic communication, user data per job	76 Byte
S7 communication	✓
S7 communication as server	✓
S7 communication as client	-
S7 communication, user data per job	160 Byte
Number of connections, max.	16
Functionality Sub-D interfaces	
Type	MP²I
Type of interface	RS485
Connector	Sub-D, 9-pin, female
Electrically isolated	-
MPI	✓
MP²I (MPI/RS232)	✓
Point-to-point interface	-
Type	COM1
Type of interface	RS232
Connector	Sub-D, 9-pin, male
Electrically isolated	-
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	✓

Order no.	**215-2BS03**
Type	COM2
Type of interface	RS232
Connector	Sub-D, 9-pin, male
Electrically isolated	-
MPI	-
MP²I (MPI/RS232)	-
Point-to-point interface	✓
Functionality MPI	
Number of connections, max.	16
PG/OP channel	✓
Routing	-
Global data communication	✓
S7 basic communication	✓
S7 communication	✓
S7 communication as server	✓
S7 communication as client	-
Transmission speed, min.	19.2 kbit/s
Transmission speed, max.	187.5 kbit/s
Point-to-point communication	
PtP communication	✓
Interface isolated	-
RS232 interface	✓
RS422 interface	-
RS485 interface	-
Connector	Sub-D, 9-pin, male
Transmission speed, min.	150 bit/s
Transmission speed, max.	115.2 kbit/s
Cable length, max.	15 m
Point-to-point protocol	
ASCII protocol	✓
STX/ETX protocol	✓
3964(R) protocol	✓
RK512 protocol	✓
USS master protocol	-
Modbus master protocol	-
Modbus slave protocol	-
Special protocols	-
Datasizes	
Input bytes	0
Output bytes	0
Parameter bytes	3
Diagnostic bytes	0
Housing	
Material	PPE / PA 6.6
Mounting	Profile rail 35 mm
Mechanical data	
Dimensions (WxHxD)	50.8 x 76 x 80 mm
Weight	150 g
Environmental conditions	
Operating temperature	0 °C to 60 °C
Storage temperature	-25 °C to 70 °C
Certifications	
UL508 certification	yes

Chapter 3 Deployment CPU 21x-2BS03

Overview

This chapter describes the deployment of the CPU in the System 200V. The description refers directly to the CPU and to the deployment in connection with peripheral modules, mounted on a profile rail together with the CPU at the backplane bus.

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Assembly

Note!

Information about assembly and cabling may be found at chapter "Basics and Assembly".

Start-up behavior

Turn on power supply

When the CPU is delivered it has been reset. After the power supply has been switched on, the CPU changes to the operating mode the operating mode lever shows. After a STOP→RUN transition the CPU switches to RUN without program.

Note!

Due to a long storage of the CPU, the battery may be discharged excessively. Please connect the CPU at least for 24 hours to the power supply, to achieve the full buffer capacity.

Boot procedure with valid data in the CPU

The CPU switches to RUN with the program stored in the battery buffered RAM.

Boot procedure with empty battery

The accumulator/battery is automatically loaded via the integrated power supply and guarantees a buffer for max. 30 days. If this time is exceeded, the battery may be totally discharged. This means that the battery buffered RAM is deleted.

In this state, the CPU executes an overall reset because with an empty battery the RAM content is undefined. If a MMC with a S7PROG.WLD is plugged, program code and data blocks are transferred from the MMC into the work memory of the CPU.

If there is no MMC, the project from the internal Flash is loaded.

Depending on the position of the operating mode switch, the CPU remains in STOP respectively switches to RUN. Due to the battery error the CPU can only boot if there was an OB81 configured. Otherwise a manual restart (STOP/RUN) respectively PG command is necessary.

On a start-up with an empty battery the SF LED is on and thus points to an entry in the diagnostic buffer. Information about the Event-IDs can be found at "VIPA specific diagnostic entries".

Attention!

After a power reset and with an empty battery the CPU starts with a BAT error and executes an overall reset.

Addressing

Automatic addressing

To provide specific addressing of the installed peripheral modules, certain addresses must be allocated in the CPU.

The CPU contains a peripheral area (addresses 0 ... 1023) and a process image of the inputs and the outputs (for both each address 0 ... 127).

When the CPU is initialized it automatically assigns peripheral addresses to the digital input/output modules starting from 0.

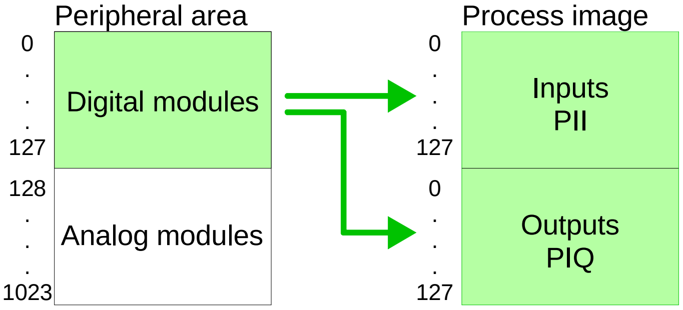
If there is no hardware projecting, analog modules are allocated to even addresses starting from address 128.

Signaling states in the process image

The signaling states of the lower addresses (0 ... 127) are additionally saved in a special memory area called the *process image*.

The process image is divided into two parts:

- process image of the inputs (PII)
- process image of the outputs (PIQ)



The process image is updated automatically when a cycle has been completed.

Read/write access

You may access the modules by means of read or write operations on the peripheral bytes or on the process image.

Note!

Please remember that you may access different modules by means of read and write operations on the same address.

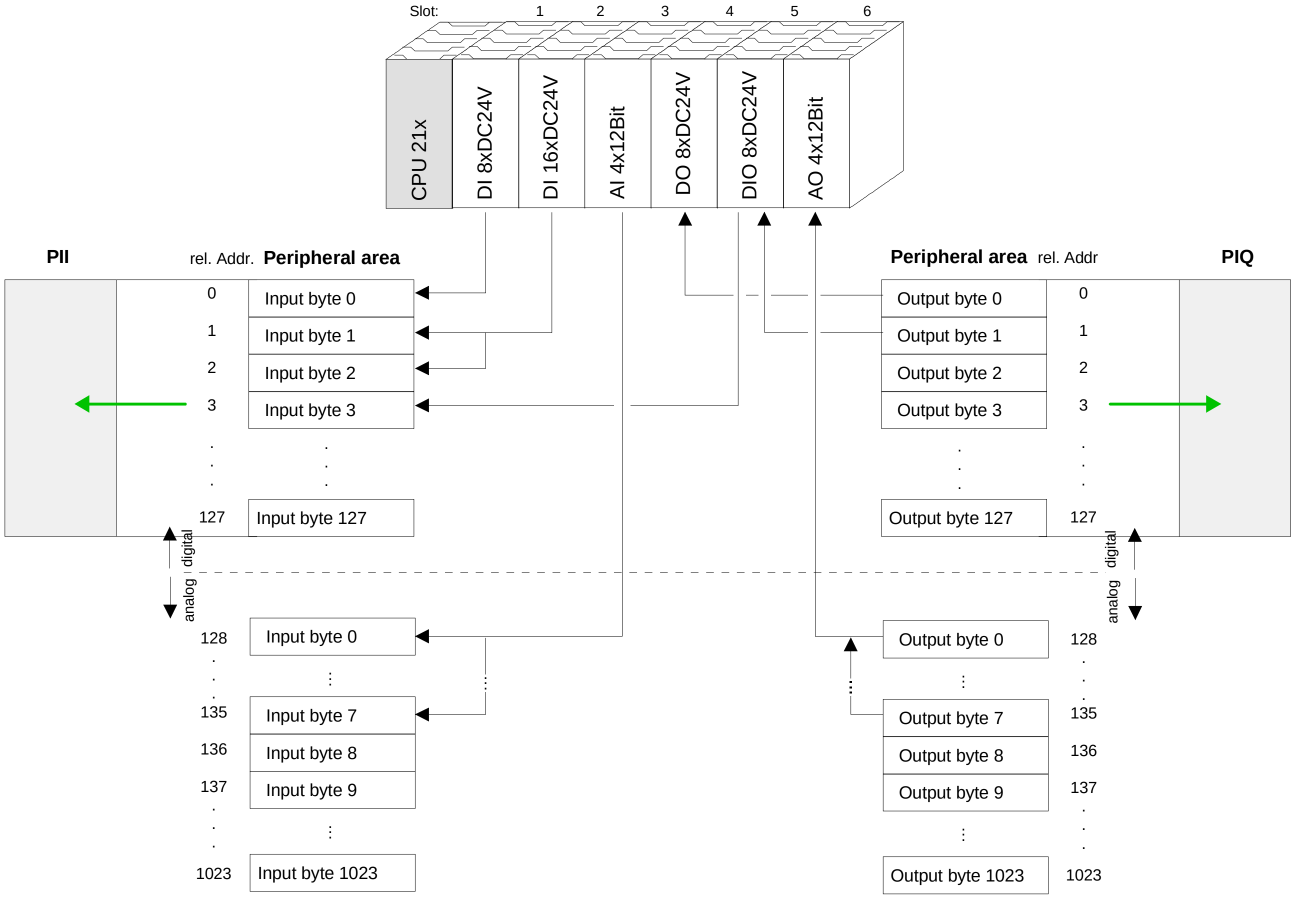
The addressing ranges of digital and analog modules are different when they are addressed automatically.

Digital modules: 0 ... 127

Analog modules: 128 ... 1023

Example for automatic address allocation

The following figure illustrates the automatic allocation of addresses:



Modifying allocated addresses by configuration

You may change the allocated addresses at any time by means of the Siemens SIMATIC manager. In this way you may also change the addresses of analog modules to the range covered by the process image (0 ... 127) and address digital modules above 127.

The following pages describe the required preparations and the procedure for this type of configuration.

Hints for the deployment of the MPI interface

What is MP^{2}I?

The MP^{2}I jack combines 2 interfaces in 1:

- MP interface
- RS232 interface

Please regard that the RS232 functionality is only available by using the Green Cable from VIPA.

Deployment as MP interface

The MP interface provides the data transfer between CPUs and PCs. In a bus communication you may transfer programs and data between the CPUs interconnected via MPI.

Connecting a common MPI cable, the MPI jack supports the full MPI functionality.

⚠

Important notes for the deployment of MPI cables!

Deploying MPI cables at the CPUs from VIPA, you have to make sure that Pin 1 is not connected. This may cause transfer problems and in some cases damage the CPU!

Especially PROFIBUS cables from Siemens, like e.g. the 6XV1 830-1CH30, must not be deployed at MP^{2}I jack.

For damages caused by nonobservance of these notes and at improper deployment, VIPA does not take liability!

Deployment as RS232 interface only via "Green Cable"

For the serial data transfer from your PC, you normally need a MPI transducer. Fortunately you may also use the "Green Cable" from VIPA. You can order this under the order no. VIPA 950-0KB00.

The "Green Cable" supports a serial point-to-point connection for data transfer via the MP^{2}I jack exclusively for VIPA CPUs.

Hardware configuration - CPU

Overview

For the project engineering of the CPU 21x and the other System 200V modules connected to the same VIPA bus, the hardware configurator from Siemens is to be used.

To address the directly plugged peripheral modules, you have to assign a special address in the CPU to every module.

The address allocation and the parameterization of the modules takes place in the Siemens SIMATIC manager as a virtual PROFIBUS system. For the PROFIBUS interface is standardized software sided, the functionality is guaranteed by including a GSD-file into the Siemens SIMATIC manager.

Transfer your project into the CPU via the MPI interface.

Requirements

The following conditions must be fulfilled for project engineering:

- The Siemens SIMATIC manager is installed at PC respectively PU
- The GSD files have been included in Siemens hardware configurator
- Serial connection to the CPU (e.g. MPI-Adapter)

Note!

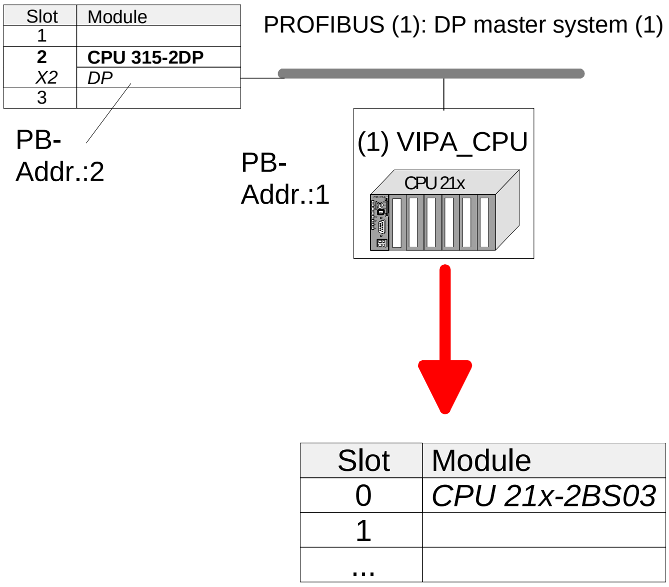
The configuration of the CPU requires a thorough knowledge of the Siemens SIMATIC manager and the hardware configurator!

Including the GSD-file

- Go to www.vipa.com > Service > Download > PROFIBUS GSD files and download the file *System_100V_-_200V_Vxxx.zip*.
- Extract the file to your work directory. The vipa_21x.gsd (German) respectively vipa_21x.gse (English) can be found at the directory *CPU21x*.
- Start the Siemens hardware configurator and close every project.
- Go to **Options** > *Install new GSD file*
- Navigate to the directory *CPU21x* and choose the corresponding file **vipa_21x.gsd** (German) or **vipa_21x.gse** (English)

Now the modules of the VIPA System 200V are integrated in the hardware catalog at *PROFIBUS-DP \ Additional field devices \ I/O \ VIPA_System_200V*.

Proceeding To be compatible with the Siemens SIMATIC manager the following steps should be executed:



Slot	Module
1	
2	**CPU 315-2DP**
X2	*DP*
3	

Slot	Module
0	*CPU 21x-2BS03*
1	
...	

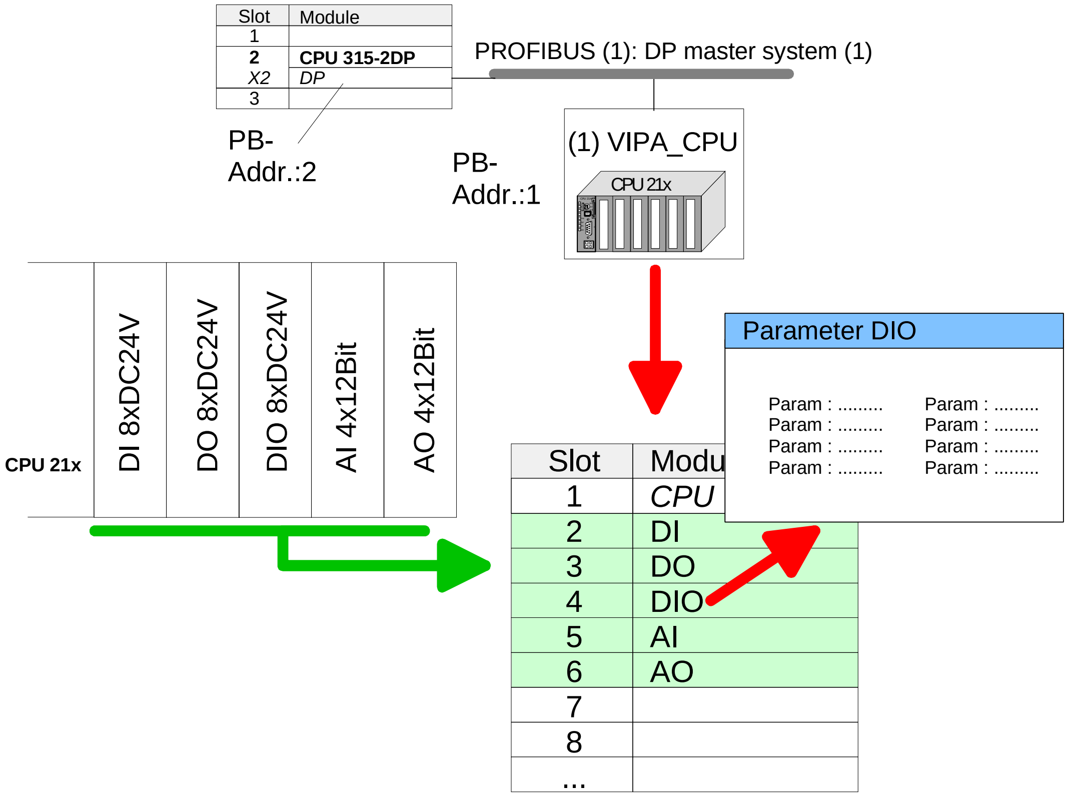
- Start the hardware configurator from Siemens with a new project.
- Insert a profile rail from the hardware catalog.
- Place at slot 2 the following CPU from Siemens:
  CPU 315-2DP (315-2AF03 0AB00 V1.2)
- For the System 200V create a new PROFIBUS subnet.
- Attach the slave system "VIPA_CPU21x" to the subnet with **PROFIBUS-Address 1**.
  After installing the vipa_21x.gsd the slave system may be found at the hardware catalog at PROFIBUS DP > Additional field devices > IO > VIPA_System_200V.
- Place **always at the 1. slot** the corresponding CPU 21x-2BS03, by taking it from the hardware catalog.

Hardware configuration - I/O modules

Hardware configuration of the modules

After the hardware configuration of the CPU place the System 200V modules in the plugged sequence.

In order to address the installed peripheral modules individually, specific addresses in the CPU have to be assigned to them.



Slot	Module
1	
2	**CPU 315-2DP**
X2	*DP*
3	

Slot	Modu
1	*CPU*
2	DI
3	DO
4	DIO
5	AI
6	AO
7	
8	
...	

Parameterization

For parameterization double-click during the project engineering at the slot overview on the module you want to parameterize. In the appearing dialog window you may set the wanted parameters.

Parameterization during runtime

By using the SFCs 55, 56 and 57 you may alter and transfer parameters for wanted modules during runtime.

For this you have to store the module specific parameters in so called "record sets".

More detailed information about the structure of the record sets is to find in the according module description.

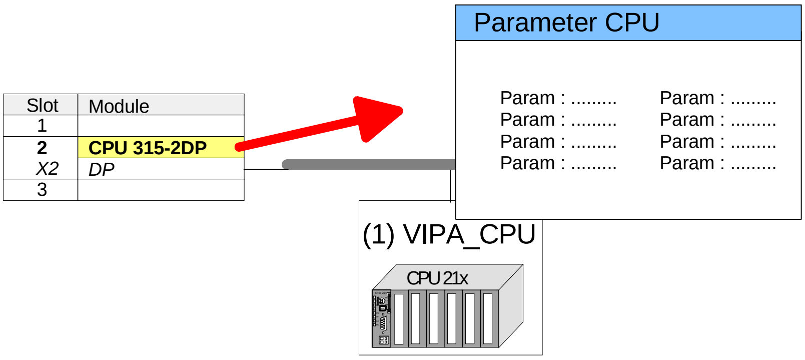
Setting CPU parameters

Parameterization via Siemens CPU 315-2AF03

Since the CPU from VIPA is to be configured as Siemens CPU 315-2DP (315-2AF03 0AB00 V1.2) in the Siemens hardware configurator, the parameters of the VIPA CPU may be set with "Object properties" of the CPU 315-2DP during hardware configuration.

Via a double-click on the CPU 315-2DP the parameter window of the CPU may be accessed.

Using the registers you get access to every standard parameter of the CPU.



Supported parameters

The CPU does not evaluate each parameter, which may be set at the hardware configuration.

The following parameters are supported by the CPU at this time:

General

Short description

The short description of the Siemens CPU 315-2AF03 is CPU 315-2DP.

Order No. / Firmware

Order number and firmware are identical to the details in the "hardware catalog" window.

Name

The *Name* field provides the *short description* of the CPU. If you change the name the new name appears in the Siemens SIMATIC manager.

Comment

In this field information about the module may be entered.

Startup

Startup when expected/actual configuration differs

If the checkbox for "Startup when expected/actual configuration differ" is *deselected* and at least one module is not located at its configured slot or if another type of module is inserted there instead, then the CPU does not switch to RUN mode and remains in STOP mode.

If the checkbox for "Startup when expected/actual configuration differ" is *selected*, then the CPU starts even if there are modules not located in their configured slots of if another type of module is inserted there instead, such as during an initial system start-up.

Monitoring time for ready message by modules [100ms]

This operation specifies the maximum time for the ready message of every configured module after PowerON. Here connected PROFIBUS DP slaves are also considered until they are parameterized. If the modules do not send a ready message to the CPU by the time the monitoring time has expired, the actual configuration becomes unequal to the preset configuration.

Monitoring time for transfer of parameters to modules [100ms]

The maximum time for the transfer of parameters to parameterizable modules. If not every module has been assigned parameters by the time this monitoring time has expired; the actual configuration becomes unequal to the preset configuration.

Cycle/Clock memory

Update OB1 process image cyclically

This parameter is not relevant.

Scan cycle monitoring time

Here the scan cycle monitoring time in milliseconds may be set. If the scan cycle time exceeds the scan cycle monitoring time, the CPU enters the STOP mode. Possible reasons for exceeding the time are:

- Communication processes
- a series of interrupt events
- an error in the CPU program

Minimum scan cycle time

This parameter is not relevant.

Scan cycle load from Communication

Using this parameter you can control the duration of communication processes, which always extend the scan cycle time so it does not exceed a specified length.

If the cycle load from communication is set to 50%, the scan cycle time of OB 1 can be doubled. At the same time, the scan cycle time of OB 1 is still being influenced by asynchronous events (e.g. hardware interrupts) as well.

OB85 call up at I/O access error

The preset reaction of the CPU may be changed to an I/O access error that occurs during the update of the process image by the system.
The VIPA CPU is preset such that OB 85 is not called if an I/O access error occurs and no entry is made in the diagnostic buffer either.

Clock memory

Activate the check box if you want to use clock memory and enter the number of the memory byte.

Note!

The selected memory byte cannot be used for temporary data storage.

Retentive Memory

Number of Memory Bytes from MB0
Enter the number of retentive memory bytes from memory byte 0 onwards.

Number of S7 Timers from T0
Enter the number of retentive *S7 timers* from T0 onwards. Each *S7 timer* occupies 2bytes.

Number of S7 Counters from C0
Enter the number of retentive *S7 counter* from C0 onwards.

Areas
These parameters are not relevant.

Interrupts

Priority
Here the priorities are displayed, according to which the hardware interrupt OBs are processed (hardware interrupt, time-delay interrupt, async. error interrupts).

Time-of-day interrupts

Priority
Here the priorities may be specified according to which the time-of-day interrupt is processed.

With priority "0" the corresponding OB is deactivated.

Active
Activate the check box of the time-of-day interrupt OBs if these are to be automatically started on complete restart.

Execution
Select how often the interrupts are to be triggered. Intervals ranging from every minute to yearly are available. The intervals apply to the settings made for *start date* and *time*.

Start date / time
Enter date and time of the first execution of the time-of-day interrupt.

Process image partition
This parameter is not supported.

Cyclic interrupts

Priority
Here the priorities may be specified according to which the corresponding cyclic interrupt is processed. With priority "0" the corresponding interrupt is deactivated.

Execution

Enter the time intervals in ms, in which the watchdog interrupt OBs should be processed. The start time for the clock is when the operating mode switch is moved from STOP to RUN.

Phase offset

Enter the delay time in ms for current execution for the watch dog interrupt. This should be performed if several watchdog interrupts are enabled. Phase offset allows to distribute processing time for watchdog interrupts across the cycle.

Process image partition

This parameter is not supported.

Protection

Level of protection

Here 1 of 3 protection levels may be set to protect the CPU from unauthorized access.

Protection level 1 (default setting):

- No password adjustable, no restrictions

Protection level 2 with password:

- Authorized users: read and write access
- Unauthorized user: read access only

Protection level 3:

- Authorized users: read and write access
- Unauthorized user: no read and write access

Project transfer

Overview

There are the following possibilities for project transfer into the CPU:

- Transfer via MPI
- Transfer via MMC when using a MMC programmer

Transfer via MPI

The structure of a MPI net is electrically identical with the structure of a PROFIBUS net. This means the same rules are valid and you use the same components for the build-up. The single participants are connected with each other via bus interface plugs and PROFIBUS cables. Per default the MPI net runs with 187.5kbaud. VIPA CPUs are delivered with MPI address 2.

MPI programming cable

The MPI programming cables are available at VIPA in different variants. The cables provide a RS232 res. USB plug for the PC and a bus enabled RS485 plug for the CPU.

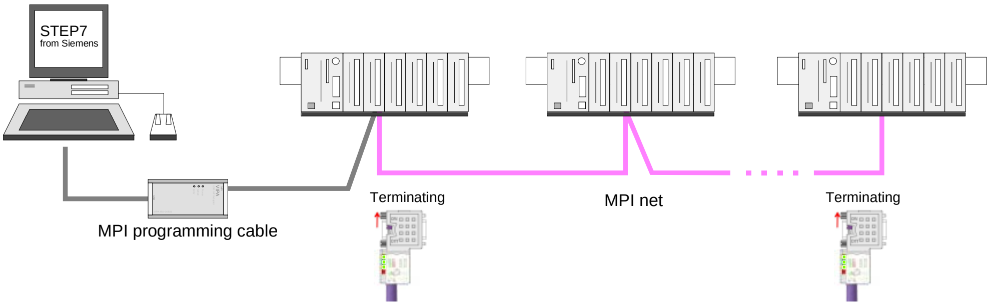
Due to the RS485 connection you may plug the MPI programming cables directly to an already plugged plug on the RS485 jack. Every bus participant identifies itself at the bus with an unique address, in the course of the address 0 is reserved for programming devices.

Terminating resistor

A cable has to be terminated with its surge impedance. For this you switch on the terminating resistor at the first and the last participant of a network or a segment.

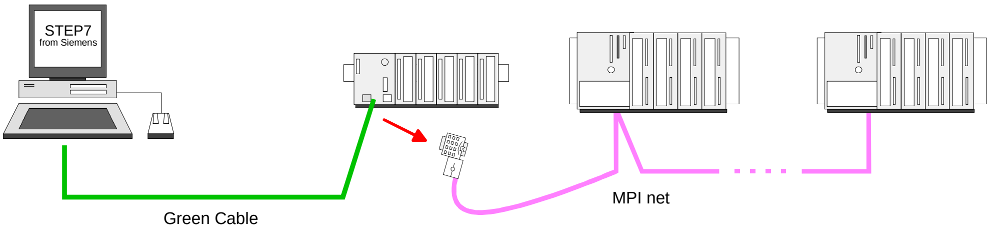
Please make sure that the participants with the activated terminating resistors are always power supplied. Otherwise it may cause interferences on the bus.

Transfer with MPI programming cable (MPI communication)



Transfer via Green Cable (serial communication)

Via exclusively direct plugging of the Green Cable to a MP^{2}I jack you may establish a serial connection between PC and CPU. Set the PC-COM port and the transfer rate 38400Baud at *Local port*. The settings of the register *MPI* are ignored at employment of the Green Cable.



Configure MPI

Hints for configuring a MPI interface are to find in the documentation of your programming software.

The "Green Cable" has the order number VIPA 950-0KB00.

Attention!

Please regard, that you may use the "Green Cable" exclusively at VIPA CPUs with MP^{2}I-interface!

Please regard the hints for deploying the Green Cable and the MP^{2}I jack!

Approach transfer via MPI interface

- Connect your PC to the MPI jack of your CPU via a MPI programming cable.
- Load your project in the SIMATIC manager from Siemens.
- Choose in the menu **Options** > *Set PG/PC interface*
- Select in the according list the "PC Adapter (MPI)"; if appropriate you have to add it first, then click on [Properties].
- Set in the register *MPI* the transfer parameters of your MPI net and type a valid *address*.
- Switch to the register *Local connection*
- Set the COM port of the PC and the transfer rate 38400Baud for the MPI programming cable from VIPA.
- Via **PLC** > *Load to module* you may transfer your project via MPI to the CPU and save it on a MMC via **PLC** > *Copy RAM to ROM* if one is plugged.

Note!

Please make sure to adjust the transfer rate to 38400Baud when using the "Green Cable" from VIPA.

Hints for the Green Cable

The Green Cable is a green connection cable, manufactured exclusively for the deployment at VIPA System components.

The Green Cable is a programming and download cable for VIPA CPUs MP^{2}I jack and VIPA field bus masters. The Green Cable from VIPA is available under the order no. VIPA 950-0KB00.

The Green Cable allows you to:

- *transfer projects serial*
  Avoiding high hardware needs (MPI transducer, etc.) you may realize a serial point-to-point connection via the Green Cable and the MP^{2}I jack. This allows you to connect components to your VIPA-CPU that are able to communicate serial via a MPI adapter like e.g. a visualization system.
- *execute firmware updates of the CPUs and field bus masters*
  Via the Green Cable and an upload application you may update the firmware of all recent VIPA CPUs with MP^{2}I jack and certain field bus masters (see Note).

⚠

Important notes for the deployment of the Green Cable

Nonobservance of the following notes may cause damages on system components.

For damages caused by nonobservance of the following notes and at improper deployment, VIPA does not take liability!

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Note to the application area

The Green Cable may exclusively deployed directly at the concerning jacks of the VIPA components (in between plugs are not permitted). E.g. a MPI cable has to be disconnected if you want to connect a Green Cable.

At this time, the following components support Green Cable:

VIPA CPUs with MP^{2}I jack and field bus masters from VIPA.

⚠

Note to the lengthening

The lengthening of the Green Cable with another Green Cable res. The combination with further MPI cables is not permitted and causes damages of the connected components!

The Green Cable may only be lengthened with a 1:1 cable
(all 9 pins are connected 1:1).

Transfer via MMC

The MMC (**Mem**ory **C**ard) serves as external transfer and storage medium. There may be stored several projects and sub-directories on a MMC storage module. Please regard that your current project is stored in the root directory and has one of the following file names:

- *S7PROG.WLD*
- *S7PROGF.WLD*
- *AUTOLOAD.WLD*

With **File** > *Memory Card File* > *New* in the Siemens SIMATIC manager a new wld file may be created. After the creation copy the blocks from the project blocks folder and the *System data* into the wld file.

Transfer MMC → CPU

The transfer of the application program from the MMC into the CPU takes place depending on the file name after an overall reset or PowerON.

- *S7PROG.WLD* is read from the MMC after overall reset and transferred into the battery buffered RAM.
- *S7PROGF.WLD* is read from the MMC after overall reset and transferred into the battery buffered RAM and additionally into the Flash memory. An access to the Flash memory only takes place at empty battery of the buffer and when no MMC with user program is plugged-in.
- *AUTOLOAD.WLD* is read after PowerON from the MMC and transferred into the battery-buffered RAM .

During the transfer the "MC" LED blinks. Please regard that your user memory serves for enough space, otherwise your user program is not completely loaded and the SF LED gets on. Execute a compression before the transfer, for this does not happen automatically.

Transfer CPU → MMC

When the MMC has been installed, the write command stores the content of the battery buffered RAM as *S7PROG.WLD* on the MMC and in the internal Flash memory.

The write command is controlled by means of the block area of the Siemens SIMATIC manager **PLC** > *Copy RAM to ROM*. During the write process the "MC"-LED of the CPU is blinking. When the LED expires the write process is finished.

If this project is to be loaded automatically from the MMC with PowerON, you have to rename this on the MMC to *AUTOLOAD.WLD*.

Transfer control

After a MMC access, an ID is written into the diagnostic buffer of the CPU. To monitor the diagnosis entries, you select **PLC** > *Module Information* in the Siemens SIMATIC manager. Via the register "Diagnostic Buffer" you reach the diagnosis window.

Information about the Event-IDs can be found at "VIPA specific diagnostic entries".

Operating modes

Overview

The CPU can be in one of 3 operating modes:

- Operating mode STOP
- Operating mode START-UP
- Operating mode RUN

Certain conditions in the operating modes START-UP and RUN require a specific reaction from the system program. In this case the application interface is often provided by a call to an organization block that was included specifically for this event.

Operating mode STOP

- The application program is not processed.
- If there has been a processing before, the values of counters, timers, flags and the process image are retained during the transition to the STOP mode.
- Outputs are inhibited, i.e. all digital outputs are disabled.
- RUN-LED (R) off
- STOP-LED (S) on

Operating mode START-UP

- During the transition from STOP to RUN the system calls the start-up organization block OB 100. The processing time for this OB is not monitored. The start-up OB may issue calls to other blocks.
- All digital outputs are disabled during the start-up, i.e. outputs are inhibited.
- RUN-LED blinks as soon as the OB 100 is operated and for at least 3s, even if the start-up time is shorter or the CPU gets to STOP due to an error. This indicates the start-up.
- STOP-LED off

When the CPU has completed the start-up OB, it assumes the operating mode RUN.

Operating mode RUN

- The application program in OB 1 is processed in a cycle. Under the control of alarms other program sections can be included in the cycle.
- All timers and counters being started by the program are active and the process image is updated with every cycle.
- The BASP-signal (outputs inhibited) is deactivated, i.e. all digital outputs are enabled.
- RUN-LED on
- STOP-LED off

Function security

The CPUs include security mechanisms like a watchdog (100ms) and a parameterizable cycle time surveillance (parameterizable min. 1ms) that stop res. execute a RESET at the CPU in case of an error and set it into a defined STOP state.

The VIPA CPUs are developed function secure and have the following system properties:

Event	concerns	Effect
RUN → STOP	general	BASP (**B**efehls-**A**usgabe-**Sp**erre, i.e. command output lock) is set.
	central digital outputs	The outputs are disabled.
	central analog outputs	The Outputs are disabled. - Voltage outputs issue 0V - Current outputs 0...20mA issue 0mA - Current outputs 4...20mA issue 4mA If configured also substitute values may be issued.
	decentral outputs	Same behavior as the central digital/analog outputs.
	decentral inputs	The inputs are cyclically be read by the decentralized station and the recent values are put at disposal.
STOP → RUN res. PowerON	general	First the PII is deleted, then OB 100 is called. After the execution of the OB, the BASP is reset and the cycle starts with: Delete PIO → Read PII → OB 1.
	central analog outputs	The behavior of the outputs at restart can be preset.
	decentral inputs	The inputs are cyclically be read by the decentralized station and the recent values are put at disposal.
RUN	general	The program execution happens cyclically and can therefore be foreseen: Read PII → OB 1 → Write PIO.

PII = Process image inputs

PIO = Process image outputs

Overall reset

Overview

During the overall reset the entire user memory is erased. Data located in the memory card is not affected.

You have 2 options to initiate an overall reset:

- initiate the overall reset by means of the function selector switch
- initiate the overall reset by means of the configuration software e.g. Siemens SIMATIC manager

Note!

You should always issue an overall reset to your CPU before loading an application program into your CPU to ensure that all blocks have been cleared from the CPU.

Overall reset by means of the function selector

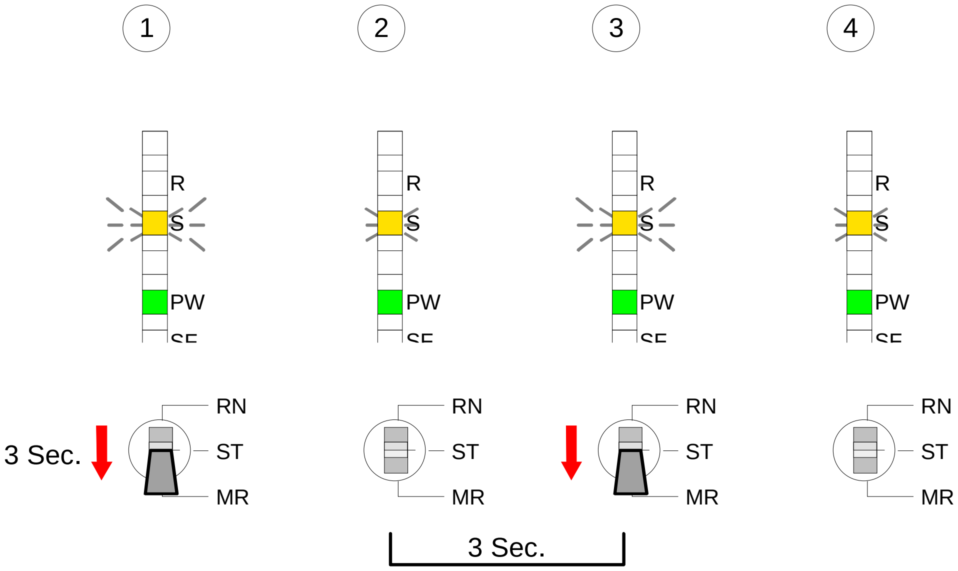
Condition

The operating mode of the CPU is STOP. Place the function selector on the CPU in position "ST" → the S-LED is on.

Overall reset

- Place the function selector in the position MR and hold it in this position for app. 3 seconds. → The S-LED changes from blinking to permanently on.
- Place the function selector in the position ST and switch it to MR and quickly back to ST within a period of less than 3 seconds. → The S-LED blinks (overall reset procedure).
- The overall reset has been completed when the S-LED is on permanently. → The S-LED is on.

The following figure illustrates the above procedure:



Automatic reload

If there is a project S7PROG.WLD on the MMC, the CPU attempts to reload this project from MMC → the MC LED is on.

When the reload has been completed the LED is extinguished. The operating mode of the CPU will be STOP or RUN, depending on the position of the function selector.

Overall reset by means of the Siemens SIMATIC manager

Condition

The operating mode of the CPU must be STOP.
You may place the CPU in STOP mode by the menu command **PLC** > *Operating mode*.

Overall reset

You may request the overall reset by means of the menu command **PLC** > *Clean/Reset*.

In the dialog window you may place your CPU in STOP mode and start the overall reset if this has not been done as yet.

The S-LED blinks during the overall reset procedure.

When the S-LED is on permanently the overall reset procedure has been completed.

Automatic reload

At this point the CPU attempts to reload the parameters and the program from the memory card. → The MC LED is on.

When the reload has been completed, the LED expires. The operating mode of the CPU will be STOP or RUN, depending on the position of the function selector.

Reset to factory setting

A *Factory reset* deletes the internal RAM of the CPU completely and sets it back to the delivery state.

Please regard that the MPI address is also set back to default 2!

More information may be found at the part "Factory reset" further below.

Firmware update

Overview

There is the opportunity to execute a firmware update for the CPU and its components via MMC. For this an accordingly prepared MMC must be in the CPU during the startup.

So a firmware files can be recognized and assigned with startup, a file name is reserved for each updateable component (see table below).

After PowerON and CPU STOP the CPU checks if there is a firmware file on the MMC. If this firmware version is different to the existing firmware version, this is indicated by blinking of the LEDs and the firmware may be installed by an update request.

Latest Firmware at www.vipa.com

The latest firmware versions are to be found in the service area at www.vipa.com

Find out CPU firmware version

A label on the rear of the module indicates the firmware version.

You may display the current firmware version of your CPU via the Siemens SIMATIC manager. To display the firmware version, you go online with the CPU via your PG or PC and start the Siemens SIMATIC manager.

Via **PLC** > *Module status,* register "General", the current firmware version is evaluated and displayed.

Load firmware and transfer it to MMC with reserved file name

- Go to www.vipa.com
- Click on Service > Download > Firmware.
- Navigate to via System 200V > CPU to your CPU and download according to your hardware version the zip file to your PC.
- Open the zip file and copy the bin file to your MMC.
- Rename this accordingly

Reserved file names

By means of a reserved file name in the CPU 21x-2BS03 you may transfer a firmware per MMC:

Component	File name order no._release_version.ZIP	New file name at MMC
CPU	Bx000... .bin	firmware.bin

Attention!

When installing a new firmware you have to be extremely careful. Under certain circumstances you may destroy the CPU, for example if the voltage supply is interrupted during transfer or if the firmware file is defective.

In this case, please call the VIPA-Hotline!

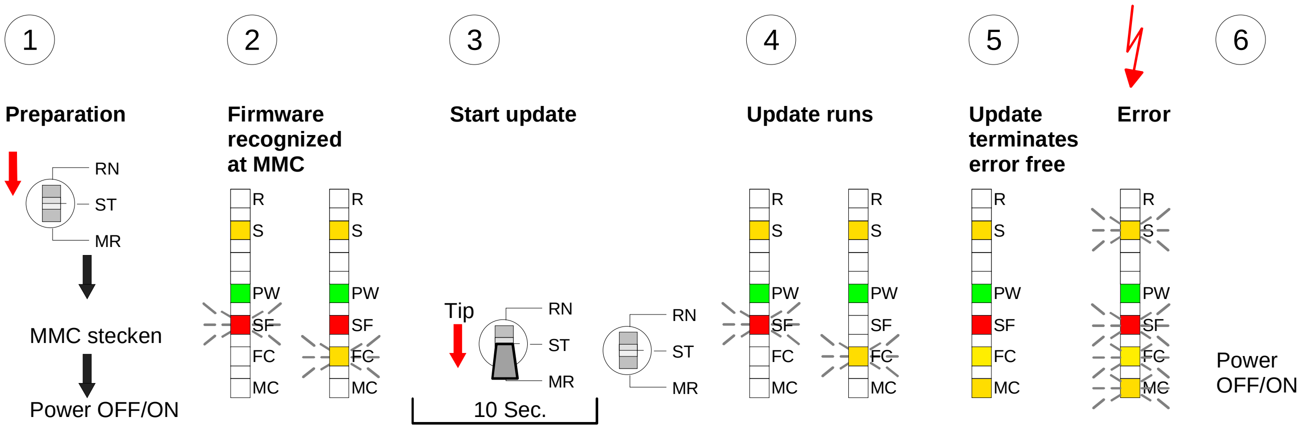
Please regard that the version of the update firmware has to be different from the existing firmware otherwise no update is executed.

Transfer firmware from MMC into CPU

1. Switch the operating mode switch of your CPU in position ST. Turn off the voltage supply. Plug the MMC with the firmware files into the CPU. Please take care of the correct plug-in direction of the MMC. Turn on the voltage supply.
2. After a short boot-up time, the alternate blinking of the LEDs SF and FC shows that at least a differing firmware file was found on the MMC.
3. You start the transfer of the firmware as soon as you tip the operating mode switch lever downwards to MR within 10s and leave it in ST position.
4. During the update process, the LEDs SF and FC are alternately blinking and MC LED is on. This may last several minutes.
5. The update is successful finished when the LEDs PW, S, SF, FC and MC are on. If they are blinking fast, an error occurred.
6. Turn Power OFF and ON. Now it is checked by the CPU, whether further current firmware versions are available at the MMC. If so, again the LEDs SF and FC flash after a short start-up period. Continue with point 3.

   If the LEDs do not flash, the firmware update is ready.

   Now a *factory reset* should be executed (see next page). After that the CPU is ready for duty.



Factory reset

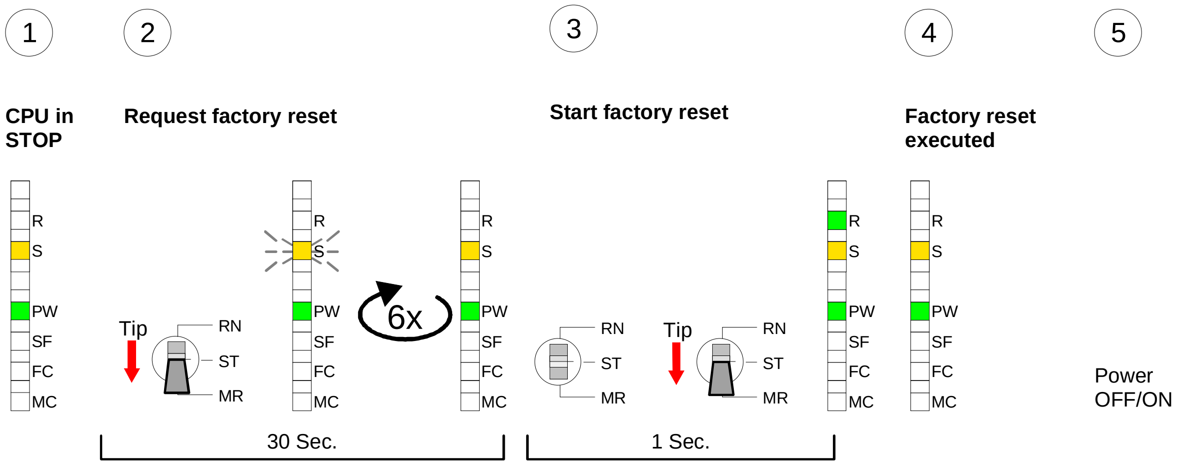
Proceeding

With the following proceeding the internal RAM of the CPU is completely deleted and the CPU is reset to delivery state.

Please note that here also the MPI address is reset to the address 2!

1. Switch the CPU to STOP.
2. Push the operating mode switch down to position MR for 30s. Here the S LED flashes. After a few seconds the stop LED changes to static light. Now the S LED changes between static light and flashing. Starting here count the static light states of the S LED.
3. After the 6. static light release the operating mode switch and tip it downwards to MR. Now the RUN LED lights up once. This means that the RAM was deleted completely.
4. For the confirmation of the resetting procedure the LEDs PW and S are on.
5. Then you have to switch the power supply off and on.

The proceeding is shown in the following Illustration:



Note!

After the firmware update you always should execute a *Factory reset*.

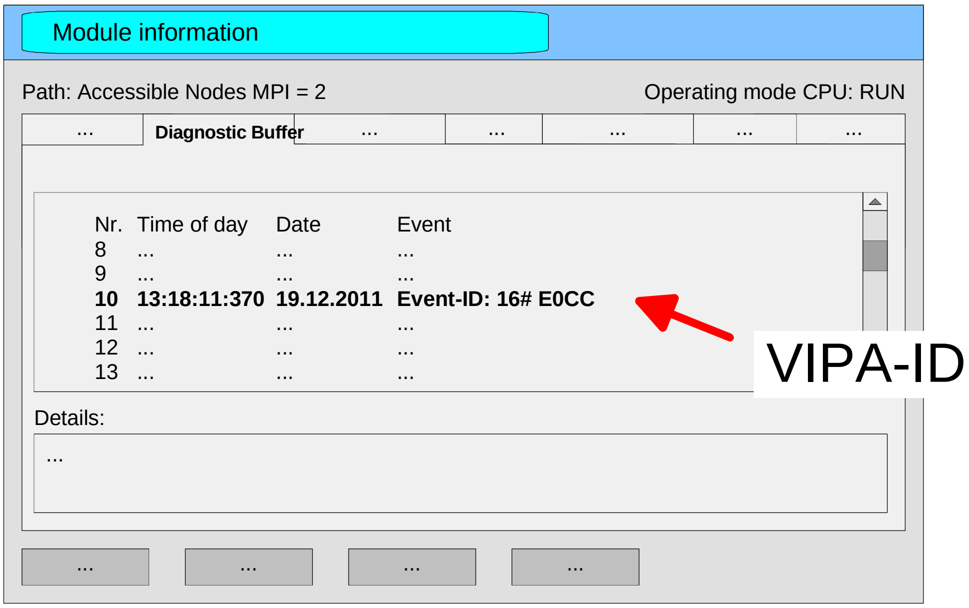
VIPA specific diagnostic entries

Entries in the diagnostic buffer

You may read the diagnostic buffer of the CPU via the Siemens SIMATIC manager. Besides of the standard entries in the diagnostic buffer, the VIPA CPUs support some additional specific entries in form of event-IDs.

Monitoring the diagnostic entries

To monitor the diagnostic entries you choose the option **PLC** > *Module Information* in the Siemens SIMATIC manager. Via the register "Diagnostic Buffer" you reach the diagnostic window:



Path: Accessible Nodes MPI = 2

Operating mode CPU: RUN

Nr.	Time of day	Date	Event
8	...	...	...
9	...	...	...
10	**13:18:11:370**	**19.12.2011**	**Event-ID: 16# E0CC**
11	...	...	...
12	...	...	...
13	...	...	...

The diagnosis is independent from the operating mode of the CPU. You may store a max. of 100 diagnostic entries in the CPU.

The following page shows an overview of the VIPA specific Event-IDs.

Overview of the Event-IDs

Event-ID	Description
0xE003	Error at access to I/O devices Zinfo1: I/O address Zinfo2: Slot
0xE004	Multiple parameterization of a I/O address Zinfo1: I/O address Zinfo2: Slot
0xE005	Internal error – Please contact the VIPA-Hotline!
0xE006	Internal error – Please contact the VIPA-Hotline!
0xE007	Configured in-/output bytes do not fit into I/O area
0xE008	Internal error – Please contact the VIPA-Hotline!
0xE009	Error at access to standard back plane bus
0xE010	Not defined module group at backplane bus recognized Zinfo2: Slot Zinfo3: Type ID
0xE011	Master project engineering at Slave-CPU not possible or wrong slave configuration
0xE012	Error at parameterization
0xE013	Error at shift register access to VBUS digital modules
0xE014	Error at Check_Sys
0xE015	Error at access to the master Zinfo2: Slot of the master (32=page frame master)
0xE016	Maximum block size at master transfer exceeded Zinfo1: I/O address Zinfo2: Slot
0xE017	Error at access to integrated slave
0xE018	Error at mapping of the master I/O devices
0xE019	Error at standard back plane bus system recognition
0xE01A	Error at recognition of the operating mode (8 / 9 Bit)
0xE0CC	Communication error MPI / Serial
0xE100	MMC access error
0xE101	MMC error file system
0xE102	MMC error FAT
0xE104	MMC error at saving
0xE200	MMC writing finished (Copy Ram to Rom)
0xE210	MMC reading finished (reload after overall reset)
0xE300	Internal Flash writing ready (Copy RAM to ROM)
0xE310	Internal Flash reading finished (reload after battery failure)

Using test functions for control and monitoring of variables

Overview

For troubleshooting purposes and to display the status of certain variables you can access certain test functions via the menu item **Debug** of the Siemens SIMATIC manager.

The status of the operands and the VKE can be displayed by means of the test function **Debug** > *Monitor*.

You can modify and/or display the status of variables by means of the test function **PLC** > *Monitor/Modify Variables*.

Debug > *Monitor*

This test function displays the current status and the VKE of the different operands while the program is being executed.

It is also possible to enter corrections to the program.

Note!
When using the test function “Monitor” the PLC must be in RUN mode!

The processing of the states may be interrupted by means of jump commands or by timer and process-related alarms. At the breakpoint the CPU stops collecting data for the status display and instead of the required data it only provides the PG with data containing the value 0.

For this reason, jumps or time and process alarms can result in the value displayed during program execution remaining at 0 for the items below:

- the result of the logical operation VKE
- Status / AKKU 1
- AKKU 2
- Condition byte
- absolute memory address SAZ. In this case SAZ is followed by a "?".

The interruption of the processing of statuses does not change the execution of the program. It only shows that the data displayed is no longer.

PLC > *Monitor/Modify Variables*

This test function returns the condition of a selected operand (inputs, outputs, flags, data word, counters or timers) at the end of program-execution.

This information is obtained from the process image of the selected operands. During the "processing check" or in operating mode STOP the periphery is read directly from the inputs. Otherwise only the process image of the selected operands is displayed.

Control of outputs

It is possible to check the wiring and proper operation of output-modules.

You can set outputs to any desired status with or without a control program. The process image is not modified but outputs are no longer inhibited.

Control of variables

The following variables may be modified:

I, Q, M, T, C and D.

The process image of binary and digital operands is modified independently of the operating mode of the CPU.

When the operating mode is RUN the program is executed with the modified process variable. When the program continues they may, however, be modified again without notification.

Process variables are controlled asynchronously to the execution sequence of the program.

Chapter 4 Serial communication

Overview

Content of this chapter is the usage of the serial RS232 interface of the CPU. Here you'll find all information about the deployment of the serial interfaces of the CPU.

Content

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Fast introduction

General

The CPU 21x-2BS03 provide serial interfacing facilities between the processes of different source and destination systems. The CPU has got 2 serial RS232 interfaces.

The communication happens via handling blocks that are stored in the CPU as library.

Protocols

The CPU supports the ASCII, STX/ETX, 3964(R) and RK512 protocols.

Parameterization

For the parameter transfer to the communication processor (CP), you have to execute SEND (SFC 230) with order no. 201 during runtime. For this you store the parameters in a DB where the structure depends on the wanted protocol.

To activate the parameters, you execute a RESET (SFC 234) with order no. 0 after the SEND.

Note!

Please regard that the commands SEND, RECEIVE, FETCH and RESET require a preceding "RLO"=1 (**r**esult of **l**ogic **o**peration) otherwise they are not executed.

Communication

The internal CP of the CPU 21x-2BS03 is directly connected to the CPU part via a Dual-Port-RAM, also called "page frame". This page frame is available at the CPU section as standard CP interface. The data transfer happens via the standard handling blocks (SEND, RECEIVE and FETCH).

The communication via the according protocols is controlled by connection commands that are programmed in the user application.

The following SFCs are used:

SFC	Name	Description
SFC 230	SEND	Send via page frame (page frame comm.)
SFC 231	RECEIVE	Receive via page frame (page frame comm.)
SFC 232	FETCH	Fetch via page frame (page frame comm.)
SFC 233	CONTROL	Control for page frame communication
SFC 234	RESET	Reset for page frame communication
SFC 235	SYNCHRON	Synchron for page frame communication
SFC 236	SEND_ALL	Send_All via page frame (page frame comm.)
SFC 237	RECV_ALL	Receive_All via page frame (page frame com.)

Depending to the protocol the following handling blocks are used:

ASCII	STX/ETX 3964(R)	RK512	SFC	Name
x	x	x	SFC 230	SEND
x	x		SFC 231	RECEIVE
		x	SFC 232	FETCH
x	x	x	SFC 233	CONTROL
x	x	x	SFC 234	RESET
x	x	x	SFC 235	SYNCHRON
x	x	x	SFC 236	SEND_ALL
x	x	x	SFC 237	RECV_ALL

Protocols and Procedures

Overview

The CPU supports the following protocols and Procedures:

- ASCII communication
- STX/ETX
- 3964(R) with RK512

ASCII

ASCII data communication is one of the simple forms of data exchange. Incoming characters are transferred 1 to 1.

To ensure that messages can be divided into logical parts the 'character delay time‘ (ZVZ) of the receiver must be matched by the transmitter. The ZVZ is specified in milliseconds (ms) and it must be larger than or equal to 2ms.

On the transmitter the equivalent of the receiver's character delay time is the 'time from reception of job ‘ (ZNA). These two times can be used to establish a simple serial PLC communication path. Any transmit job is only acknowledged with 'job completed without errors' (AFOF) when the data was transmitted and the ZNA has expired.

If ZNA is set to 0, the send sequence has to be controlled via the user application.

STX/ETX

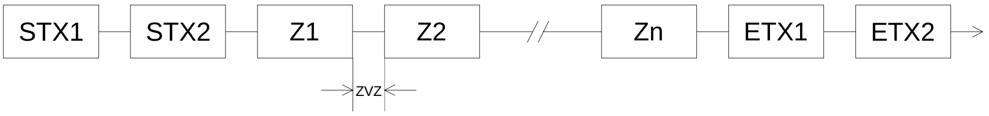
STX/ETX is a simple protocol with start and end ID, where STX stands for **S**tart of **T**e**x**t and ETX for **E**nd of **T**e**x**t.

The STX/ETX procedure is suitable for the transfer of ASCII characters (20h…7Fh). It does not use block checks (BCC). Any data transferred from the periphery must be preceded by an Start followed by the data characters and the end character.

The effective data which includes all the characters between Start and End are transferred to the CPU when the End has been received.

When data is send from the CPU to a peripheral device, any user data is handed to the CPU where transferred to the communication partner.

Message structure:



You may define up to 2 start and end characters.

You may work with 1, 2 or no Start- and with 1, 2 or no End-ID. As Start- res. End-ID all Hex values from 01h to 1Fh are permissible. Characters above 1Fh are ignored. In the user data, characters below 20h are not allowed and may cause errors. The number of Start- and End-IDs may be different (1 Start, 2 End res. 2 Start, 1 End or other combinations). If no End-ID is defined, all read characters are transferred to the CPU after a parameterizable character delay time (Timeout).

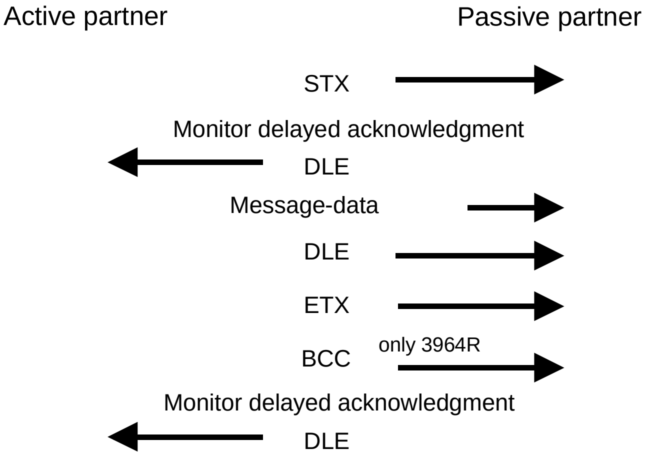
3964(R)

The 3964(R) procedure controls the data transfer of a point-to-point link between the CPU 21x-2BS03 and a communication partner. The procedure adds control characters to the message data during data transfer. These control characters may be used by the communication partner to verify the complete and error free receipt.

The procedure employs the following control characters:

• STX	**S**tart of **Tex**t
• DLE	**D**ata **L**ink **E**scape
• ETX	**E**nd of **T**ext
• BCC	**B**lock **C**heck **C**haracter (only at 3964R)
• NAK	**N**egative **Ac**knowledge

Procedure



You may transfer a maximum of 255Byte per message.

Note!

When a DLE is transferred as part of the information it is repeated to distinguish between data characters and DLE control characters that are used to establish and to terminate the connection (DLE duplication). The DLE duplication is reversed in the receiving station.

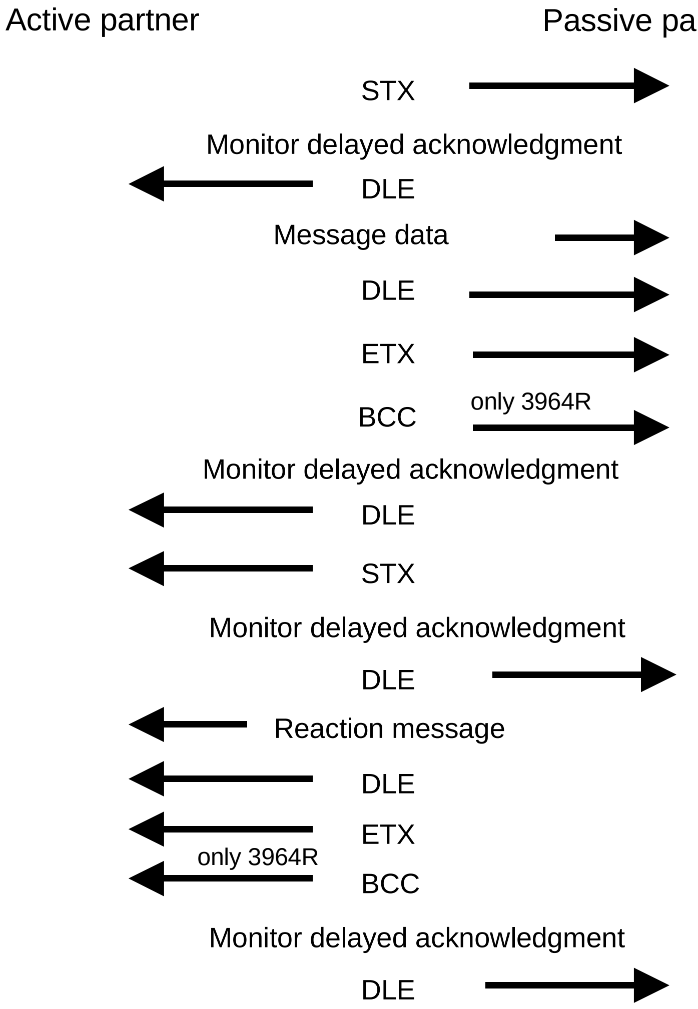
The 3964R procedure requires that a lower priority is assigned to the communication partner. When communication partners issue simultaneous send commands, the station with the lower priority will delay its send command.

3964(R) with RK512

The RK512 is an extended form of the 3964(R) procedure. The difference is that a message header is sent ahead of the message data. The header contains data about the size, type and length of the message data.

Procedure

The following paragraph describes the structure of the procedure and messages:


Active partner
Passive partner
STX
Monitor delayed acknowledgment
DLE
Message data
DLE
ETX
BCC
only 3964R
Monitor delayed acknowledgment
DLE
STX
Monitor delayed acknowledgment
DLE
Reaction message
DLE
ETX
only 3964R
BCC
Monitor delayed acknowledgment
DLE

Coordination flags

The coordination flag is set in the partner PLC in active-mode when a message is being received. This occurs for input as well as for output commands. When the coordination flag has been set and a message with this flag is received, then the respective data is not accepted (or transferred) and a reject message is sent (error code 32h). In this case the user has to reset the coordination flag in the partner PLC.

If you want to transfer telegrams without coordination flag, you have to set FFFFh.

Timeout times

The following time-outs apply :

Acknowledgement delay time:	(QVZ)	=	2000 ms
Character delay time:	(ZVZ)	=	220 ms

The QVZ is monitored between STX and DLE and between BCC and DLE. ZVZ is monitored for the entire period of receiving the message.

When the QVZ expires after an STX, the STX is repeated. This process is repeated 3*) times after which the attempt to establish a connection is terminated by the transmission of a NAK. The same sequence is completed when a NAK or any other character follows an STX.

When the QVZ expires after a message (following the BCC-byte) or when a character other than DLE is received the attempt to establish the connection and the message are repeated. This process is also repeated 3*) times after which a NAK is transmitted and the attempt is terminated.

*) adjustable via parameter

Passive operation

When the procedure driver is expecting a connection request and it receives a character that is not equal to STX it will transmit a NAK. The driver does not respond with an answer to the reception of a NAK.

When ZVZ expires during the reception, the driver will send a NAK and wait for another connection request.

The driver also sends a NAK when it receives an STX while it is not ready.

Block-Check-character (BCC-Byte)

The 3964R procedure appends a Block check character to safeguard the transmitted data. The BCC-Byte is calculated by means of an XOR function over the entire data of the message, including the DLE/ETX.

When a BCC-Byte is received that differs from the calculated BCC, a NAK is transmitted instead of the DLE.

Initialization conflict

If two stations should simultaneously attempt to issue a connection request within the QVZ then the station with the lower priority will transmit the DLE and change to receive mode.

DLE

The driver duplicates any DLE-character that is contained in a message, i.e. the sequence DLE/DLE is sent. During the reception, the duplicated DLEs are saved as a single DLE in the buffer. The message always terminates with the sequence DLE/ETX/BCC (only for 3964R).

The control codes :	02h = STX
	03h = ETX
	10h = DLE
	15h = NAK

RS232 interface

Properties

- Interface compatible to the COM interface of a PC
- Protocols supported: ASCII, STX/ETX, 3964(R) and RK512
- Receive buffer of 1024Byte and send buffer with 1024Byte
- The maximum telegram length is 1024Byte

Properties of the RS232 interface

- Logical signals as voltage levels
- Point-to-point links with serial full-duplex transfer in 3-wire technology with data transfers over distances of up to 15m
- Data transfer rate up to 57.6kBaud

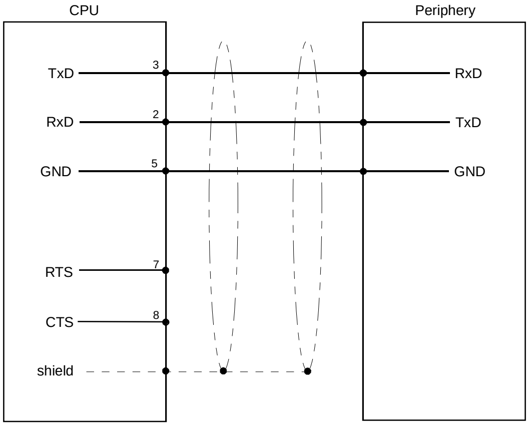
Connection interface

Via 9pin plug, you may establish a serial point-to-point connection.

9pin plug

Pin	Description
1	CD-
2	RxD
3	TxD
4	DTR-
5	GND
6	DSR-
7	RTS-
8	CTS-
9	RI-

Connection RS232



The CPU 21x-2BS03 currently supports the following RS232 signals:

TxD Transmit Data

The transmit data is transferred via the TxD line. When the transmit line is not used the CPU 21x-2BS03 holds it at a logical "1".

RxD Receive Data

The receive data arrives via the RxD line. When the receive line is not in use, it must be held at a logical "1" by the transmitting station.

Communication

Overview

Data communication is controlled by means of the handler blocks.

The CPU decides the type of data transfer depending on the parameterization. The standard modes use the SEND/RECEIVE blocks for order initialization and the "ALL" blocks for the user data communication.

The following blocks are supplied:

SFC	Label	Description
SFC 235	SYNCHRON	Synchronization between CPU and CP and presetting of the block size
SFC 230	SEND	Initialize a send order
SFC 236	SEND-ALL	Send user data
SFC 231	RECEIVE	Initialize a receive order
SFC 237	RECEIVE-ALL	Receive user data
SFC 232	FETCH	Initialize a fetch order
SFC 233	CONTROL	Block for communication control
SFC 234	RESET	Deletes all orders and activates new parameter

Depending to the protocol the following handling blocks are used:

ASCII	STX/ETX 3964(R)	RK512	SFC	Name
x	x	x	SFC 230	SEND
x	x		SFC 231	RECEIVE
		x	SFC 232	FETCH
x	x	x	SFC 233	CONTROL
x	x	x	SFC 234	RESET
x	x	x	SFC 235	SYNCHRON
x	x	x	SFC 236	SEND_ALL
x	x	x	SFC 237	RECV_ALL

Programming

The following text shows the approach of programming in easy steps:

Start-up OB100:

- Call SYNCHRON with SFC 235 and enter the wanted block size (Page frame basic address=0, Block size, PAFE)
- Parameterize the interfaces with SEND (SFC 230) with order no. 201 and parameter DB
- To take over the parameters, you call RESET (SFC 234) with order no. 0

Cycle OB1:

- Create SEND and RECEIVE orders for send and receive initialization
- Create SEND ALL and RECEIVE ALL orders for user data transfer

A more detailed description follows.

Initialize interfaces

Overview

The initialization of the interfaces happens in OB 100 and should be executed with the following approach:

- Call SYNCHRON with SFC 235 and enter the wanted block size (page frame basic address=0, block size, PAFE)
- Parameterize the interfaces via SEND (SFC 230) with order no. 201 and parameter DB
- To take over the parameters, call RESET (SFC 234) with order no. 0

SFC 235 SYNCHRON

The SYNCHRON block initializes the synchronization between CPU and CP during the boot process and for this it has to be called in the start-up OB 100. Simultaneously the transition area of the interface is deleted and predefined and the CP and the CPU agree about the block size.

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
BLGR	IN	INT	Block size
PAFE	OUT	BYTE	Parameterization error

SSNR

Number of the logical interface (page frame address) to which the according order refers to. SSNR must be 0!

Block size

To avoid long cycle run-times it is convenient to split large data amounts into smaller blocks for transmitting them between CP and CPU. You declare the size of this blocks by means of "block size".

A large block size = high data throughput, but also longer run-times and therefore a high cycle time strain.

A small block size = smaller data throughput, but also shorter run-times of the blocks.

Following block sizes are available:

Value	*Block size*	*Value*	*Block size*
0	Default (64Byte)	4	128Byte
1	16Byte	5	256Byte
2	32Byte	6	512Byte
3	64Byte	255	512Byte

Parameter type : Integer

Valid range : 0 ... 255

Example

```
CALL  SFC  235
SSNR:=0
BLGR:=6
PAFE:=MB199
```

SFC 230 - SEND with ANR=201 and Parameter-DB

You may transfer parameters to the CP via SEND (SFC 230), ANR=201 and DB.

Please regard that a send command is only executed when the following conditions are met:

- the SEND has received a RLO "1"
- the Bit "order in process" in the indicator word has been reset

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
IND	IN	INT	Mode of addressing
QANF	IN	ANY	Pointer to data source
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word

SFC 234 - RESET

A RESET with order number 0 interrupts all orders and the previous parameters are activated.

Analog to SEND, the block requires a preceding RLO=1.

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
PAFE	OUT	BYTE	Parameterization error

Example OB100

```
CALL  SFC  235                SYNCHRON
SSNR:=0
BLGR:=6
PAFE:=MB199

SET                           RLO=1
CALL  SFC  230                SEND: parameter for COM1
SSNR:=0
ANR :=201                     ID for parameterization
IND :=0
QANF:=P#DB9.DBX0.0 BYTE 20    Pointer to parameter for COM1
PAFE:=MB198
ANZW:=MD200

SET                           RLO=1
CALL  SFC  230                SEND: parameter for COM2
SSNR:=0
ANR :=201                     ID for parameterization
IND :=0
QANF:=P#DB9.DBX20.0 BYTE 20   Pointer to parameter for COM2
PAFE:=MB198
ANZW:=MD200

SET                           RLO=1
CALL  SFC  234                RESET
SSNR:=0
ANR :=0                       ID for RESET
PAFE:=MB197
```

Interface parameters

Parameter-DB structure

The parameter transfer to the communication processor happens during runtime by using the SFC 230 with order no. 201. The parameters for the protocols have to be stored in a DB.

To activate the parameters you have to execute a RESET with SFC 234 after transfer.

General parameters for every channel in use:

Data byte	Type	Designator		Values	Default
0	BYTE	Channel	COM 1 COM 2	1 2	
1	BYTE	Mode	MODI_NONE (deactivated) MODI_1 (Parameter following)	0 81h	0
2	BYTE	Baudrate	BAUDRATE_DEF BAUDRATE_150 BAUDRATE_300 BAUDRATE_600 BAUDRATE_1K2 BAUDRATE_1K8 BAUDRATE_2K4 BAUDRATE_4K8 BAUDRATE_7K2 BAUDRATE_9K6 BAUDRATE_14K4 BAUDRATE_19K2 BAUDRATE_38K4 BAUDRATE_57K6	00h 01h 02h 03h 04h 05h 06h 07h 08h 09h 0Ah 0Bh 0Ch 0Dh	09h
3	BYTE	DataBits	DATABIT_5 DATABIT_6 DATABIT_7 DATABIT_8	0 1 2 3	3
4	BYTE	Parity	PARITY_NONE PARITY_ODD PARITY_EVEN	0 1 3	0
5	BYTE	StopBits	STOPBIT_1 STOPBIT_1_5 STOPBIT_2	1 2 3	1
6	BYTE	FlowControl	FLOW_NONE FLOW_HARDWARE FLOW_XON_XOFF	0 1 2	1
7	BYTE	Protocol	PROTOCOL_ASCII PROTOCOL_STXETX_HTB PROTOCOL_3964 PROTOCOL_3964R PROTOCOL_3964_RK512 PROTOCOL_3964R_RK512	01h 02h 03h 04h 05h 06h	01h

Additional parameters depending on the protocol

Depending on the selected protocol the following parameters must also be specified in the DB:

if PROTOCOL_ASCII:

Data byte	Type	Designator	Values	Default
Transmit channel				
8, 9	WORD	BufAnz	1 ... n	1
10, 11	WORD	BufSize	16 ... 1024	256
12, 13	WORD	ZNA, time delay after job	0 ... n	500
Receive channel				
14, 15	WORD	BufAnz	1 ... n	1
16, 17	WORD	BufSize	16 ... 1024	256
18, 19	WORD	ZVZ, character delay time	2 ... n	200

if PROTOCOL_STXETX:

Data byte	Type	Designator	Values	Default
Transmit channel				
8, 9	WORD	BufAnz	1 ... n	1
10, 11	WORD	BufSize	16 ... 1024	256
12, 13	WORD	ZNA, time delay after job	0 ... n	0
Start code				
14, 15	WORD	Quantity	1, 2	1
16	BYTE	Code 1	0 ... 255	STX
17	BYTE	Code 2	0 ... 255	STX
End code				
18, 19	WORD	Quantity	1, 2	1
20	BYTE	Code 1	0 ... 255	ETX
21	BYTE	Code 2	0 ... 255	ETX
Receive channel				
22, 23	WORD	BufAnz	1 ... n	1
24, 25	WORD	BufSize	16 ... 1024	256
26, 27	WORD	TMO, Timeout	2 ... n	200
Start code				
28, 29	WORD	Quantity	1, 2	1
30	BYTE	Code 1	0 ... 255	STX
31	BYTE	Code 2	0 ... 255	STX
End code				
32, 33	WORD	Quantity	1, 2	1
34	BYTE	Code 1	0 ... 255	ETX
35	BYTE	Code 2	0 ... 255	ETX

if PROTOCOL_3964(R):

Data byte	Type	Designator	Values	Default
Transmit-/ receive channel				
8, 9	WORD	BufAnz	1 ... n	1
10, 11	WORD	BufSize	16 ... 1024	128
12, 13	WORD	ZNA, time delay after job	0 ... n	0
14, 15	WORD	ZVZ char. delay time	1 ... n	200
16, 17	WORD	QVZ ack. delay time	1 ... n	500
18, 19	WORD	BWZ block delay time (	1 ... n	10000
20, 21	WORD	STX number of retries connection set-up	1 ... n	3
22, 23	WORD	DBL number of retries data blocks	1 ... n	6
24, 25	WORD	Priority 0==Low, >0==High	0, 1	1

if PROTOCOL_3964(R)_RK512:

Data byte	Type	Designator	Values	Default
Transmit-/ receive channel				
8, 9	WORD	BufAnz	1 ... n	1
10, 11	WORD	BufSize	16 ... 1024	128
12, 13	WORD	ZNA, time delay after job	0 ... n	0
14, 15	WORD	ZVZ char. delay time	1 ... n	200
16, 17	WORD	QVZ ack. delay time	1 ... n	500
18, 19	WORD	BWZ block delay time	1 ... n	10000
20, 21	WORD	STX number of retries connection set-up	1 ... n	3
22, 23	WORD	DBL number of retries data blocks	1 ... n	6
24, 25	WORD	Priority 0==Low, >0==High	0, 1	1
26, 27	WORD	QVZ for user acknowledgement	1 ... n	5000

Constant parameters

The following parameters are constants and can not be changed

Parameter	Setting
Page frame base address	0
No. of page frames	1
Job-no.	1: COM 1 SEND 2: COM 1 RECEIVE 3: COM 2 SEND 4: COM 2 RECEIVE 201: for SEND for parameterization
Job priority	2

Interface communication

Overview

The communication happens via the following handling blocks in the OB1:

No.	Designator	
SFC 230	SEND	Initialize a send order
SFC 236	SEND-ALL	Send user data
SFC 231	RECEIVE	Initialize a receive order
SFC 237	RECEIVE-ALL	Receive user data
SFC 232	FETCH	Initialize a fetch order
SFC 233	CONTROL	Block for communication control

Cycle OB1:

- Create SEND and RECEIVE orders for send and receive initialization
- Create SEND ALL and RECEIVE ALL orders for user data transfer

The following section contains a summary of this blocks.

SFC 230 - SEND

The SEND block serves the initialization of a send order to a CP.

Please regard that a send order is only executed when the following conditions are met:

- the SEND has received a RLO "1"
- the bit "order in process" in the indicator word has been reset

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
IND	IN	INT	Mode of addressing
QANF	IN	ANY	Pointer to data source
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word

SFC 236 - SEND_ALL

If the CP is able to take over the data directly, the SEND block transfers the requested data in one session. If the CP requests only the order parameters or the amount of the depending data is too large, the CP only gets the sending parameters res. the parameter with the first data block. The according data res. the assigned serials blocks for this order are requested from the CP by SEND_ALL to the CPU. For this it is necessary that the block SEND_ALL is called minimum one time per cycle.

SFC 231 - RECEIVE

The RECEIVE block receives data from a CP.

Normally the RECEIVE block is called in the cyclic part of the user application program.

For activating a RECEIVE block is only started, if:

- the RECEIVE has received a RLO "1"
- the CP released the order (bit "Handshake convenient" = 1)

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
IND	IN	INT	Mode of addressing
ZANF	IN	ANY	Pointer to data destination
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word

SFC 237 - RECEIVE_ALL

Via the RECEIVE_ALL block, the data received from the CP is transmitted from the CP to the CPU by using the declared block size.

Location and size of the data area that is to transmit with RECEIVE_ALL, must be declared before by calling RECEIVE.

In the indicator word that is assigned to the concerned order, the bit "ENABLE/DISABLE" is set, "Data transition starts" and "Data transition/fetch running" is analyzed or altered. The receiving amount is shown in the following word.

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word

Note!

In the following cases, the RECEIVE_ALL command has to be called for minimum one time per cycle of the block OB1:

- if the CP should send data to the CPU independently
- if a CP order is initialized via RECEIVE, but the CP still has to request the background communication data of the CPU for this order.
- if the amount of data, that should be transmitted to the CPU by this RECEIVE, is higher than the declared block size.

SFC 232 - FETCH

The FETCH block initializes a FETCH order in the partner station.

The FETCH order defines data source and destination and the data source is transmitted to the partner station.

The CPU from VIPA realizes the definition of source and destination via a pointer parameter.

The partner station provides the *Source* data and transmits them via SEND_ALL back to the requesting station. Via RECEIVE_ALL the data is received and is stored in *Destination*.

The update of the indicator word takes place via FETCH res. CONTROL.

Please regard that a fetch command is only executed when the following conditions are met:

- the FETCH has received a RLO "1"
- the bit "order in process" in the indicator word has been reset

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
IND	IN	INT	Mode of addressing
ZANF	IN	ANY	Pointer to data destination
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word

SFC 233 - CONTROL

The purpose of the CONTROL block is the following:

- Update of the indicator word
- Query if a certain order of the CP is currently active, e.g. request for a receipt telegram
- Query the CP which order is recently in commission.
- The block is independent from the RLO and should be called from the cyclic part of the application.

Parameters

Name	Declaration	Type	Description
SSNR	IN	INT	Interface number
ANR	IN	INT	Job number
PAFE	OUT	BYTE	Parameterization error
ANZW	IN_OUT	DWORD	Indicator word