Handbücher/Manuals

art of automation

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Manual

VIPA CPU 51xS SPEED7

Order No.: VIPA HB145E
Rev. 04/35

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Disclaimer of liability

The contents of this manual was carefully examined to ensure that it conforms with the described hardware and software.
However, discrepancies can not be avoided. The specifications in this manual are examined regularly and corrections will be included in subsequent editions.
We gratefully accept suggestions for improvement.

Trademarks

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STEP®	is a registered trademark of Siemens AG.
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Content

Outline

This product supplement contains all information required for the deployment of the Slot-PLC CPU 51xPCI in your PC.

The here described Slot-PLC is a SPEED7 CPU 51xS with integrated Profibus-DP master.

The CPU is included in the PC as Ethernet interface and can be accessed via the IP address.

Content

Order data

Type	Order number	Description
CPU 517S	VIPA 517-2AJ00	CPU 517PCI with Profibus-DP master, 1/1MB w/l memory
MMC	VIPA 953-0KX00	MMC storage module
USB-MMC reading device	VIPA 950-0AD00	USB adapter for MMC programming
Green Cable	VIPA 950-0KB00	PC/AG download cable
WinPLC7	VIPA WinPLC7	Programming tool
WinNCS	VIPA SW-WinNCS	Parameterization software for Profibus-DP under Win 95/98/NT
OPC-Server	VIPA SW860M	Driver license for MPI included with CPU 51x
	VIPA SW860T	Driver license for TCP/IP (read/write)

User considerations

Objective and contents

This manual describes the CPU 51xS with all product variants. It contains a description of the construction, project engineering and the usage.

Target audience

The manual is targeted at users who have a background in automation technology.

Structure of the manual

At present the manual consists of 20 chapters. Every chapter provides a self-contained description of a specific topic.

Guide to the document

The following guides are available in the manual:

- an overall table of contents at the beginning of the manual
- an overview of the topics for every chapter
- an index at the end of the manual.

Availability

The manual is available in:

- printed form, on paper
- in electronic form as PDF-file (Adobe Acrobat Reader)

Icons Headings

Important passages in the text are highlighted by following icons and headings:

Danger!
Immediate or likely danger.
Personal injury is possible.

Attention!
Damages to property is likely if these warnings are not heeded.

Note!
Supplementary information and useful tips.

Safety information

Applications conforming with specifications

The CPU51xS is constructed and produced for:

- the employment under Profibus
- communication and process control
- general control and automation applications
- industrial applications
- operation within the environmental conditions specified in the technical data
- installation into a cubicle

Danger!

This device is not certified for applications in

- in explosive environments (EX-zone)

Documentation

The manual must be available to all personnel in the

- project design department
- installation department
- commissioning
- operation

The following conditions must be met before using or commissioning the components described in this manual:

- Modification to the process control system should only be carried out when the system has been disconnected from power!
- Installation and modifications only by properly trained personnel
- The national rules and regulations of the respective country must be satisfied (installation, safety, EMC ...)

Disposal

National rules and regulations apply to the disposal of the unit!

Safety information for Users

Handling of electrostatically sensitive modules

VIPA modules make use of highly integrated components in MOS-technology. These components are extremely sensitive to over-voltages that can occur during electrostatic discharges.

The following symbol is attached to modules that can be destroyed by electrostatic discharges:

The symbol is located on the module, the module rack or on packing material and it indicates the presence of electrostatic sensitive equipment.

It is possible that electrostatic sensitive equipment is destroyed by energies and voltages that are far less than the human threshold of perception. These voltages can occur where persons do not discharge themselves before handling electrostatically sensitive modules and they can damage components thereby, causing the module to become inoperable or unusable. Modules that have been damaged by electrostatic discharges may fail after a temperature change, mechanical shock or changes in the electrical load.

Only the consequent implementation of protection devices and meticulous attention to the applicable rules and regulations for handling the respective equipment can prevent failures of electrostatically sensitive modules.

Shipping of electrostatically sensitive modules

Modules have to be shipped in the original packing material.

Measurements and alterations on electrostatically sensitive modules

When you are conducting measurements on electrostatically sensitive modules you should take the following precautions:

- Floating instruments must be discharged before use.
- Instruments must be grounded.

Modifying electrostatically sensitive modules you should only use soldering irons with grounded tips.

Attention!

Personnel and instruments should be grounded when working on electrostatically sensitive modules.

Hints for the deployment of the MPI interface

What is MP²I?

The MP²I jack combines 2 interfaces in 1:

- MP interface
- RS232 interface

Please regard that the RS232 functionality is only available by using the Green Cable from VIPA.

Deployment as MP interface

The MP interface provides the data transfer between CPUs and PCs. In a bus communication you may transfer programs and data between the CPUs interconnected via MPI.

Connecting a common MPI cable, the MPI jack supports the full MPI functionality.

Important notes for the deployment of MPI cables!

Deploying MPI cables at the CPUs from VIPA, you have to make sure that Pin 1 is not connected. This may cause transfer problems and in some cases damage the CPU!

Especially Profibus cables from Siemens, like e.g. the 6XV1 830-1CH30, must not be deployed at MP²I jack.

For damages caused by nonobservance of these notes and at improper employment, VIPA does not take liability!

Deployment as RS232 interface only via "Green Cable"

For the serial data transfer from your PC, you normally need a MPI transducer. Fortunately you may also use the "Green Cable" from VIPA. You can order this under the order no. VIPA 950-0KB00.

The "Green Cable" supports a serial point-to-point connection for data transfer via the MP²I jack exclusively for VIPA components.

Please regard the hints for the deployment of the "Green Cable" on the following page.

Hints for the Green Cable from VIPA

What is the Green Cable?

The Green Cable is a green connection cable, manufactured exclusively for the employment at VIPA System components.

The Green Cable is a programming and download cable for VIPA PLCs and VIPA fieldbus masters. The Green Cable from VIPA is available under the order no. VIPA 950-0KB00.

The Green Cable allows you to:

- *transfer projects serial*
  Avoiding high hardware needs (MPI transducer, etc.) you may realize a serial point-to-point connection via the Green Cable and the MP^{2}I jack.
- *execute firmware updates of the CPUs and fieldbus masters*
  Via the Green Cable and an upload application you may update the firmware of all recent CPUs 11x, 21x, 31x, 51x and certain fieldbus masters (see Note).

Important notes for the deployment of the Green Cable

Nonobservance of the following notes may cause damages on system components.

For damages caused by nonobservance of the following notes and at improper deployment, VIPA does not take liability!

Note to the application area

The Green Cable may exclusively employed directly at the concerning jacks of the VIPA components (in between plugs are not permitted).

Note to the lengthening

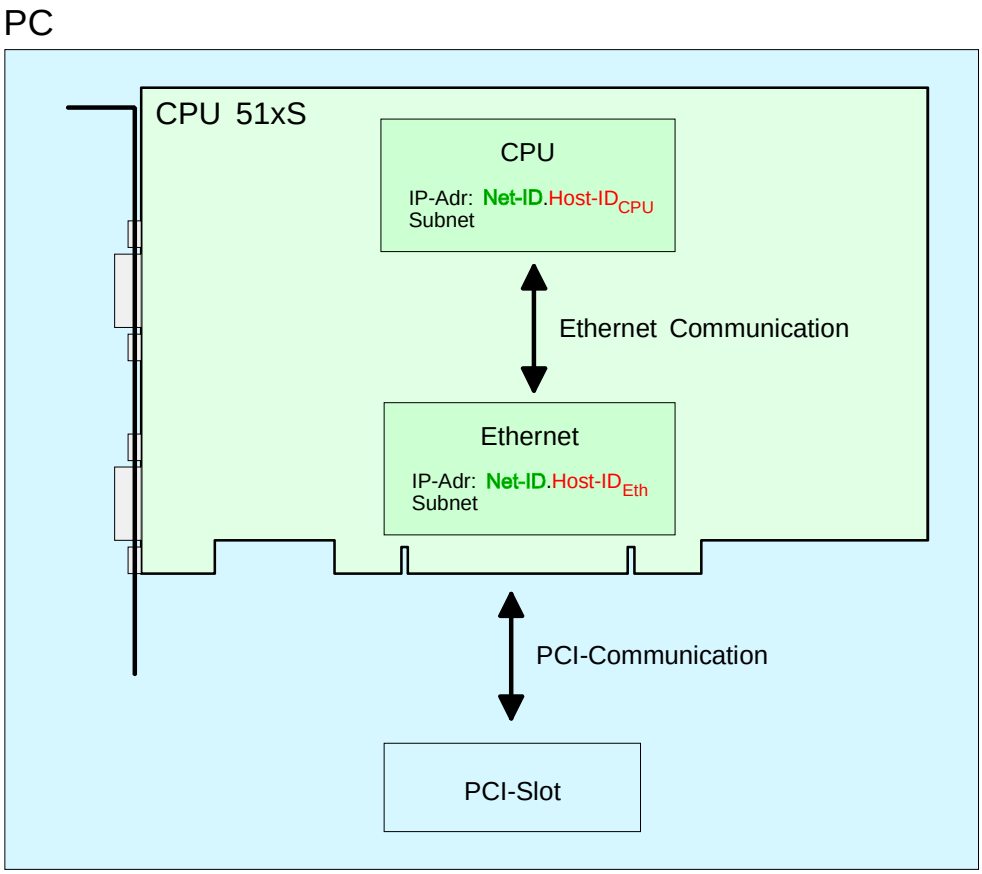
The lengthening of the Green Cable with another Green Cable res. the combination with further MPI cables is not permitted and causes damages of the connected components!

The Green Cable may only be lengthened with a 1:1 cable (all 9 Pins are connected 1:1).

Principles of Net-ID, Subnet-ID, Host-ID

Why Principles?

The CPU 51xS PC plug-in card consists of a CPU and an Ethernet portion that communicate via a TCP-based point-to-point connection. To enable this, CPU and Ethernet portion each have an alterable IP address that may only differ in the Host-ID.



If you want to install several CPU 51xS in one PC, every CPU 51xS plug-in card needs an own Net-ID.

The following text describes the approach for the assignment of IP addresses together with Net-ID and Host-ID.

Net-ID
Host-ID

Every IP address is a combination of a **Net-ID** and a **Host-ID**.

The **Net**work-ID identifies a network res. a network controller that administrates the network.

The Host-ID marks the network connections of a participant (host) to this network.

Subnet-Mask

The Host-ID can be further divided into a **Subnet-ID** and a *new* **Host-ID** by using an bit for bit AND assignment with the **Subnet-Mask**.

The area of the original Host-ID that is overwritten by 1 of the Subnet-Mask becomes the Subnet-ID, the rest is the new Host-ID.

Subnet-Mask	binary all "1"		binary all "0"
IPv4 address	Net-ID	Host-ID	
Subnet-Mask and IPv4 address	Net-ID	Subnet-ID	*new* Host-ID

A TCP-based communication via point-to-point, hub or switch connection is only possible between stations with identical Network-ID and Subnet-ID! Different area must be connected with a router.

The Subnet-Mask allows you to sort the resources after your needs. This means e.g. that every department gets an own subnet and thus does not interfere another department.

Note!

When using the CPU 51xS in your PC, the Net-ID of the CPU 51xS must not be assigned to another device. Otherwise you have to reassign the addresses.

Address classes

For IPv4 addresses there are five address formats (class A to class E) that are all of a length of 4 Byte = 32 Bit.

Class A	0	Network-ID (1+7 bit)	Host-ID (24 bit)
Class B	10	Network-ID (2+14 bit)	Host-ID (16 bit)
Class C	110	Network-ID (3+21 bit)	Host-ID (8 bit)
Class D	1110	Multicast group	
Class E	11110	Reserved	

The classes A, B and C are used for individual addresses, class D for multicast addresses and class E is reserved for special purposes.

The address formats of the classes A, B, C are only differing in the length of Network-ID and Host-ID.

Private IP networks

To build up private IP-Networks within the internet, RFC1597/1918 reserves the following address areas:

Network class	Start IP	End IP	Standard Subnet Mask
A	10.0.0.0	10.255.255.255	255.0.0.0
B	172.16.0.0	172.31.255.255	255.255.0.0
C	192.168.0.0	192.168.255.255	255.255.255.0

(The Host-ID is underlined.)

These addresses can be used as net-ID by several organizations without causing conflicts, for these IP addresses are neither assigned in the internet nor are routed in the internet.

Reserved Host-Ids

Some Host-IDs are reserved for special purposes.

Host-ID = 0	Identifier of this network, reserved!
Host-ID = maximum (binary complete 1)	Broadcast address of this network

Note!

Never choose an IP address with Host-ID=0 or Host-ID=maximum!

(e.g. for class B with Subnet Mask = 255.255.0.0, the "172.16.0.0" is reserved and the "172.16.255.255" is occupied as local broadcast address for this network.)

CPU 51xS - SPEED7

General

The CPU 51xS is a fully adequate PLC-CPU in form of a PCI-slot card for PC-based applications. The operating systems Windows® 98, ME, NT4, 2000 and XP are supported.

The range of performance is adequate to a SPEED7 CPU from the System 300S from VIPA. The programming takes place via standard programming tools like e.g. WinPLC7 from VIPA or STEP®7 from Siemens.

For the link up to the process level there is as well a MP^{2}I as a Profibus-DP master interface. Further on, the VIPA OPC-Server is included in the delivery.

After the hardware installation, the card is linked up to the PC as COM interface. For the PCI card is working independent from the PC, you have to provide it external with DC 24V.

As an independent storage medium the PCI card contains a MMC slot for customary in the trade Multi Media Cards (MMC).

Properties

The following properties are characterizing this CPU:

- Integrated SPEED7-Chip with 100k commands in 2ms and a minimum cycle time of 100µs
- Instruction compatible to STEP®7 from Siemens
- Project engineering via the STEP®7 Manager from Siemens
- Integrated supply DC 24V
- MP^{2}Interface: MPI (8 dynamic and 8 static connections with up to 1.5MBit/s) or serial point-to-point connection to external PC
- Status-LEDs for operating state and diagnosis
- Battery buffer for RAM and clock
- Integrated Profibus-DP master
- Work memory 2MByte (1 MByte for code, 1MByte for data)
- MMC-Slot for project engineering and firmware update
- 512 Timer, 512 Counter, 8192 Memory-Byte
- Firmware update only via MMC

Operating security

- External power supply of the CPU (autarkic operation)
- ESD/Burst acc. IEC 61000-4-2/IEC 61000-4-4 (up to level 3)
- Shock resistance acc. IEC 60068-2-6 / IEC 60068-2-27 (1G/12G)

Environment conditions

- Operating temperature: 0 ... +60°C
- Storage temperature: -25 ... +70°C
- Relative humidity: 5 ... 95% without condensation
- Fanless operation

Inclusion of the card as Ethernet interface

The CPU 51xS PC plug-in card consists of a CPU and an Ethernet portion. For communication, both parts have an own IP address (Ethernet address) that may only be different in the Host-ID. Thus allows you to also use several CPU 51xS in your PC.

The Die CPU portion has the following default IP address:

CPU	
Subnet-Mask	255.255.255.0
IP address	192.168.201.3

The address for the CPU component is entered via your PLC project engineering tool in form of a virtual CP 343-1.

If the „Net“ components of the STEP®7 project engineering tool from Siemens are installed, the Slot-PLC maps into your PU/PC-interface area as **Intel(R) 8255xER**.

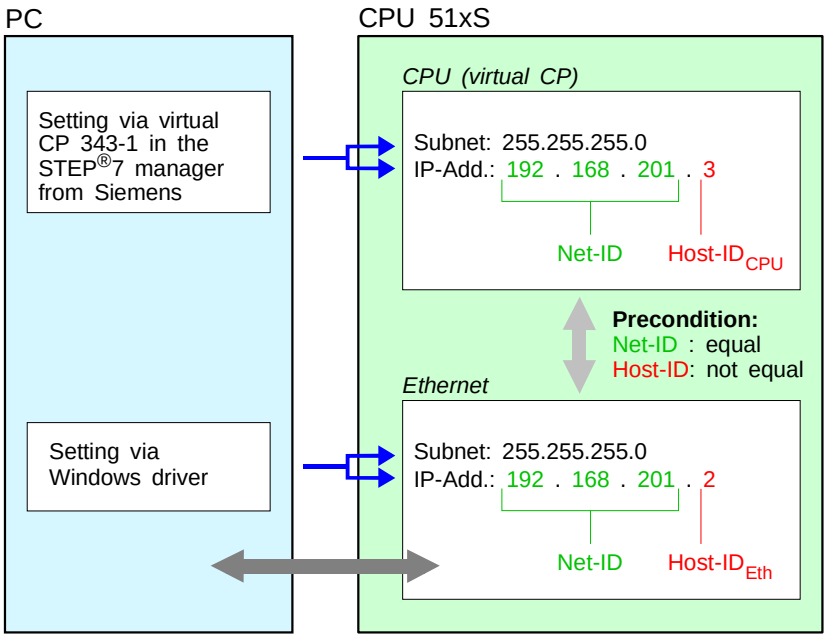
To include the plug-in card into your operating system, an according Windows driver file is in consignment. After the installation of the driver, you may enter the IP address and Subnet-Mask for the Ethernet portion of the plug-in card via the “Network environment”.

Please take care that the IP addresses of the CPU and the Ethernet component are only differing in the Host-ID.

For example, you may assign the following IP address for the Ethernet portion:

Ethernet	
Subnet-Mask	255.255.255.0
IP address	192.168.201.2

The following illustration shows the installation of the PC plug-in card:



Project engineering

The PLC 51xS is instruction compatible to STEP®7 from Siemens and may be programmed via WinPLC7 from VIPA or via the STEP®7 manager from Siemens.

An extensive function library is included in the consignment.

To be compatible to the STEP®7 project engineering tool from Siemens, the CPU51xS from VIPA must be configured as

CPU 318-2DP (6ES7 318-2AJ00-0AB0/V3.0)
with a virtual Ethernet-CP CP 343-1!

The project transfer happens internal via a virtual Ethernet interface.

For the project engineering, a thorough knowledge of the STEP®7 manager and the hardware configurator from Siemens are required!

Profibus-DP master section

For the link-up to Profibus, the CPU includes a Profibus-DP master.Via the DP master with a data range of 1kByte for in- and output you may address up to 125 DP slaves.

During the operation the DP master overlays an adjustable address area in the CPU with its own data areas. The address range is configured in your projecting tool (e.g. WinNCS from VIPA or hardware configurator from Siemens).

Project engineering of the DP master

The project engineering of the Profibus-DP master may be done under WinNCS from VIPA or in the hardware configurator from Siemens.

For accesses on the Profibus-DP master from an external PC, the MP^{2}I interface is at your disposal.

MPI connection

The CPU 51xS includes an MPI jack:

The MPI connection is lead out as MP^{2}I connection. In delivery state, the default MPI address is 2. You may alter it at any time via your CPU project engineering tool.

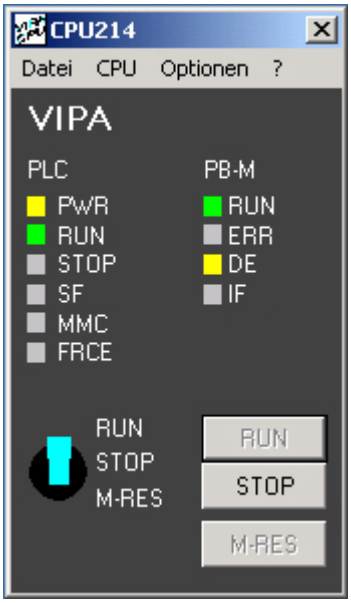
Additionally to the MPI functionality, this interface offers also the option of a serial point-to-point connection via the "Green Cable".

Please also regard the chapter "Hints for the Green Cable".

Operating options via PLC-Tool

For operating the CPU via the PC the program "PLC-Tool" is included in the consignment. For monitoring and operating of the CPU, your PC shows an user interface that is modeled on the schematic view on a CPU front.

Via the PLC-Tool you may request the LED state and monitor res. change the operating mode of the CPU.



Multi Media Card as external storage medium

CPU and Profibus-DP master are both using the Multi Media Card (MMC) as external storage medium, independent from the PC. For the installation and dismantling of the MMC you have to open the PC.

The MMC is available at VIPA.

Integrated power supply

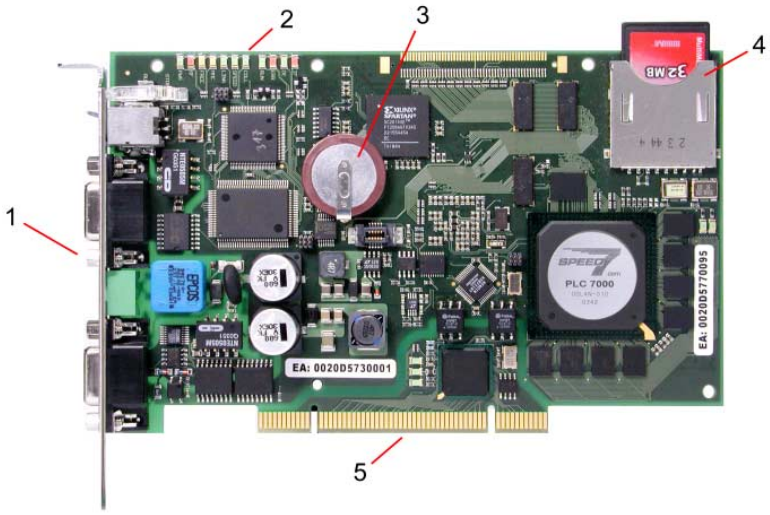
The CPU has an integrated power supply, that has to be provided with DC 24V via the front side. The power supply is protected against polarity inversion and overcurrent.

Due to the external voltage supply, you may operate your CPU 51xS card independent from the PC.

Structure

Overview

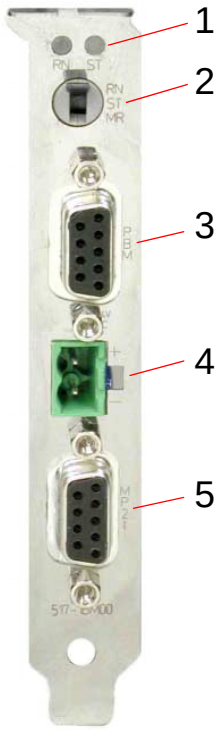
The following components are to find on the PCI slot card



[1] MP²I-, Profibus interface and port for DC 24V
[2] LEDs for commissioning
[3] Lithium accu for clock and user memory
[4] Port for MMC (here MMC is plugged)
[5] PCI-Bus pins

Plugs and jacks

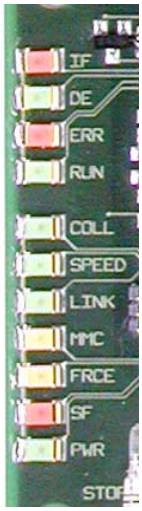
The plug-in module has the following jacks and plugs:



[1] RUN/STOP LEDs
[2] Operating mode switch
[3] Profibus-DP master jack
[4] External DC24V power supply plug
[5] MP²I jack

Components

LED bar



On the plug-in module you can see a LED bar for status monitoring of the CPU and the Profibus-DP master. Especially at the commissioning and the external usage of the module, the state of your CPU and your Profibus-DP master is shown.

At deployment inside a PC, you may issue the state of the LEDs on your PC via the delivered software PLC-Tool.

The usage and the according colors of the LEDs are to see in the following tables:

Label	Color	Description
Profibus-DP master		
IF	red	Initialization error at wrong parameterization
DE	green	DE (Data exchange) shows communication via Profibus.
ERR	red	blinks at slave break-down
RUN	green	If only RUN blinks, the DP master is in RUN. The slaves are addressed and the outputs are 0 ("clear"-state). If RUN+DE are on, the DP-Master is in "operate"-state (Data exchange with the slaves).
Ethernet		
COLL	green	Collision: on: total duplex operation active off: half duplex operation active blinking: Collision detected
SPEED	green	Speed: on: 100MBit off: 10 MBit
LINK	green	Link on: physical connection detected off: no physical connection
CPU		
MMC	yellow	blinks at MMC access
FRCE	yellow	blinks as soon as variable are forced (fixed)
SF	red	blinks at system errors (hardware defect)
PWR	yellow	CPU section is provided internal with 5V

LEDs at connection panel

Above the operating mode lever there are 2 LEDs, showing the operating state:

Label	Color	Description
STOP	yellow	CPU is in STOP
RUN	green	CPU is in RUN

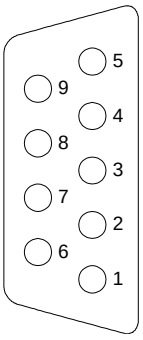
Jacks and plugs

On the PC plug-in module the following jacks are led out:

Profibus-DP master interface DPM

Via the 9pin RS485 interface you link up the integrated Profibus-DP master to Profibus. The RS485 jack has the following pin occupancy:

9-pin jack



Pin	Assignment
1	Screen
2	not used
3	RxD/TxD-P
4	CNTR-P
5	GND
6	5V (max. 70mA)
7	not used
8	RxD/TxD-N
9	not used

Note!

Please make sure to activate the terminating resistors at the bus ends!

MP²I adapter

MPI serves the connection to the process level. Here you may transfer programs and data between the MPI participants.

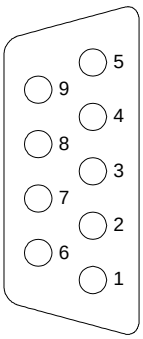
Besides the MPI functionality, the MP²I adapter also allows the serial point-to-point connection via the "Green Cable".

The "Green Cable" can exclusively be employed with VIPA components like CPUs and DP master.

Via "Green Cable" you may also parameterize the integrated Profibus-DP master.

The MP²I jack has the following pin assignment:

9-pin jack



Pin	Assignment
1	reserved
2	GND
3	RS485_A
4	RS485_CTS
5	GND_{iso}
6	Vcc
7	+24V DC
8	RS485_B
9	RS485_RTS

Port for MMC

For a PC independent backup of your project, there is a MMC port on the plug-in module.

The CPU and the integrated Profibus-DP master are both using the MMC as external storage module.

The MMC (Multi Media Card) is available at VIPA with the order number VIPA 953-0KX00.

For the MMC uses a file system, you may organize its content at the PC with the USB-MMC reading device from VIPA.

The MMC reading device has the order no.: VIPA 950-0AD00.

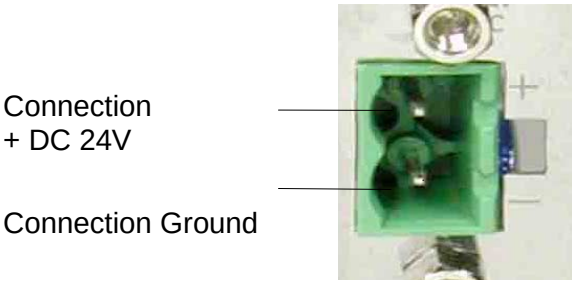
Attention!

At deployment of a MMC, please regard, that it has to be preformatted with the FAT16 file system. The VIPA MMCs are always delivered preformatted.

Voltage supply

The CPU 51xS PC plug-in card can only be operated with an external DC 24V power supply. This enables the operation of the card outside of a PC res. independent from the PC operation.

Herefore there is a plug on the connection panel with the following pin assignment:



For the cabling a plug-in jack is delivered in the consignment. For connecting your supply conductors it has got screw clamps.

Battery buffer for clock and RAM

The CPU 51xS contains an internal battery (accu) for protecting the RAM at a power break-down. Additionally the accu buffers the internal clock.

The accu is directly reloaded via the integrated voltage supply by means of a special loading electronic and guarantees a buffer of minimum 30 days.

The battery has to be error free, so the CPU may switch to RUN.

If an error occurs at the integrated accu, the CPU switches to STOP. At this event you should check the Slot-PLC card. Please contact VIPA!

First operation and start-up behavior

Note!

For the first operation and for further comprehension, a thorough knowledge of Net-ID, Host-ID and Subnet-ID are assumed. For more detailed information, please read the chapter "Principles of Net-ID, Subnet-ID, Host-ID".

When using the CPU 51xS in your PC, the Net-ID of the CPU 51xS must not already be assigned. Otherwise you must reassign the addresses. You'll find more information further below.

Network planning for the first operation

In common, your complete network consists of a PC with (at least) one network card and one or more CPU 51xS plug-in cards that are also each listed as network card with the CPU as single participant:

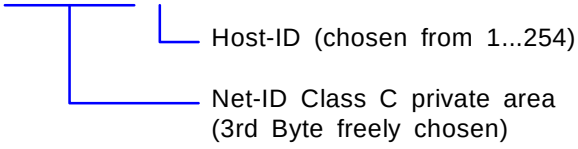
PC	
Network card (IP/Mask from DHCP-Server)	
e.g.	192.168.**1**.2 / 255.255.255.0
1. CPU 51xS	
LAN with recomm. IP/Mask	192.168.**201**.2 / 255.255.255.0
CPU with default IP/Mask	192.168.**201**.3 / 255.255.255.0
2. CPU 51xS	
LAN with new IP/Mask	192.168.**202**.2 / 255.255.255.0
CPU with new IP/Mask	192.168.**202**.3 / 255.255.255.0
3. CPU 51xS	
LAN with new IP/Mask	192.168.**203**.2 / 255.255.255.0
CPU with new IP/Mask	192.168.**203**.3 / 255.255.255.0

To enable the PC to connect the CPU 51xS plug-in cards and the subordinated CPUs without using a router table, you have to assign an **individual Net-ID** for every card!

Default configuration of the CPU 51xS at delivery

For network card and CPU, IP addresses from the private class C net have been chosen. At usage of the default subnet mask, 256 different networks with each 254 host addresses are at disposal.

CPU 51xS	
LAN with recomm. IP/Mask	192.168.**201**.2 / 255.255.255.0
CPU with default IP/Mask	192.168.**201**.3 / 255.255.255.0



Alter IP address res. subnet mask of the CPU 51xS

For the first operation, the Net-ID of the CPU 51xS plug-in card must be still available in your company network. You may need to alter the IP address res. subnet mask.

The plug-in card has 2 addresses that may only differ in the Host-ID. The presetting of the Net-ID happens for the CPU portion as PLC project, the Net-ID for the Ethernet portion is chosen in the Windows network neighborhood.

Note!

The installation of the Slot-PLC plug-in card should only be done by trained staff!

Wrong installation may cause damages at plug-in card and PC.

Steps of the first operation

Depending on the basic situation, the first operation provides the following options:

A) First operation 1 CPU 51xS plug-in card when the default Net-ID is still available in the company network:

1.	Turn off the PC.
2.	Plug the CPU 51xS plug-in card into a free PCI slot.
3.	Supply the CPU 51xS with DC24V.
4.	Turn on the PC. → The Windows operating system detects the new hardware and requests a driver.
5.	Insert the delivered VIPA driver CD and choose the according driver directory. → The **Network neighborhood** > *Properties* shows the plug-in card as additional LAN connection.
6.	Highlight the concerning LAN connection. With a right click on **Properties** > *Internet protocol TCP/IP* > *Properties* you set the default IP address = 192.168.201.2 and default Subnet Mask = 255.255.255.0. → The CPU of the plug-in card has the default IP address 192.168.201.3 and is now available from this PC via web browser or by ping to the address 192.168.201.3.

Start-up in delivery state

In delivery state, the CPU has been overall reset.

After a STOP→RUN change of the CPU, the DP master receives its parameter data.

For these are not available in an overall reset CPU, the DP master starts with its default parameters (Addr.:1, 1.5 MBit) from the ROM, shows this via the "IF"-LED and switches to RUN.

The CPU switches to RUN without application.

... Continue Steps for the first operation

B) First operation of several CPU 51xS plug-in cards where the default Net-ID is still available in the company network:

Important note!

A double assignment of the Net-ID must be avoided. At usage of several CPU 51xS PC plug-in cards, they have to be started individually one after the other!

1.	Follow the steps 1. to 6. like described under A). → For the usage of several plug-in cards, the Net-ID of the plug-in card has to be altered. The plug-in card has 2 addresses that may only differ in the Host-ID. The presetting of a Net-ID happens for the CPU portion as PLC project. The Net-ID for the Ethernet portion is set in the Windows driver.
2.	For this, connect the STEP®7 manager from Siemens via the new LAN connection to the CPU (IP address 192.168.201.3)
3.	Create a new project. Depending on the total number of Slot-PLCs in your PC, assign a **new Network-ID**, e.g. with 4 CPU 51xS plug-in cards you choose 192.168.**204**.**3** as new IP address, the subnet mask = 255.255.255.0 remains.
4.	Transfer the project into the CPU 51xS.
5.	At your desktop, you open the **Network neighborhood** > *Properties*. Here the plug-in card is shown as additional LAN connection.
6.	Highlight the concerning LAN connection. With a right click on **Properties** > *Internet protocol TCP/IP* > *Properties* you set the new IP address = 192.168.**204**.**2** and default subnet mask = 255.255.255.0. → The CPU of the plug-in card has now the IP address 192.168.204.3 and is now available from this PC via web browser or by ping to the address 192.168.204.3.
7.	Plug in another CPU 51xS plug-in card and set the Net-ID 192.168.**203** by repeating from step 1.
8.	Add more CPU 51xS plug-in cards by starting them with the default Net-ID and reassign a new Net-ID.

... Continue Steps for the first operation

C) First operation 1 CPU 51xS plug-in card where the default Net-ID is not available in the company network:

Important note!

A double assignment of the Net-ID must be avoided.

1.	If the default Net-ID is already used within your company network, you have to start the CPU 51xS PC plug-in card without connection to the according device. If this is the local network card of the PC, you should change their IP address and subnet mask temporarily.
2.	Follow the steps 1. to 6. like described under A).
3.	Enter for the CPU 51xS plug-in card a fitting IP address and subnet mask. → The plug-in card has 2 addresses that may only differ in the Host-ID. The presetting of a Net-ID happens for the CPU portion as PLC project. The Net-ID for the Ethernet portion is set in the Windows driver.
4.	For this, connect the STEP®7 manager from Siemens via the new LAN connection to the CPU (IP address 192.168.201.3)
5.	Create a new project. Assign an IP address and subnet mask fitting for your network.
6.	Transfer the project into the CPU 51xS.
7.	At your desktop, you open the **Network neighborhood** > *Properties*. Here the plug-in card is shown as additional LAN connection.
8.	Highlight the concerning LAN connection. With a right click on **Properties** > *Internet protocol TCP/IP* > *Properties* you set the IP address and subnet mask. Please regard that the IP addresses of CPU and LAN connection may only differ in the Host-ID. → For control purposes you may now reach the CPU via the CPU IP address from this PC via web browser or per ping.
9.	Now you may reconnect the “critical” component mentioned in 1. res. reset the local network card.

Hardware Configuration from the CPU 51xS

Overview

As soon as the PC plug-in card is build in and the according driver file is installed, the plug-in card is included as Ethernet interface. By choosing the "Intel"-Ethernet interface in your programming res. parameterization tool you may internally access the CPU and the Profibus master.

The integrated MPI jack allows you to transfer your project from an external programming device to the plug-in card with the “destination system functions”. In delivery state, the CPU 51xS plug-in card has the MPI address 2.

Preconditions

For the hardware configuration of the CPU and the project engineering of the integrated Profibus-DP master of the CPU, the following preconditions must be met:

- Hardware configurator from Siemens is installed
- A communication connection to the plug-in card is established
- At usage of Profibus-DP slaves of the Systems 100V, 200V and 300V from VIPA: GSD files are included in the hardware configurator.

For the project engineering of the CPU and the Profibus-DP master, a thorough knowledge of the STEP®7 manager and the hardware configurator from Siemens are assumed!

Install hardware configurator from Siemens

The hardware configurator is part of the STEP®7 configuration tool from Siemens. It serves the project engineering. The modules that you may configure here are to find in the hardware catalog.

For the deployment of Profibus slaves of the Systems 100V, 200V and 300V from VIPA, the import of the modules to the hardware catalog via the GSD-files from VIPA is necessary.

Approach

The CPU 51xS (VIPA 517-2AJ00) has to be configured analog to a CPU318-2 from Siemens with Profibus-DP master and a plugged Ethernet-CP CP343-1.

- Start the hardware configurator and create a new project System 300.
- Add a profile rail from the hardware catalog.
- You reach the CPU with Profibus master in the hardware catalog under: `Simatic300/CPU-300/CPU318-2DP/6ES7 318-2AJ00-0AB0`
- Insert the CPU 318-2DP (6ES7 318-2AJ00-0AB0/V3.0).
- Enter a Profibus address for the master (e.g. 2)
- Click on DP and set the operating mode “Master” in the *Object properties*. Confirm your entry with OK.

Configuration of the internal Ethernet connection

To enable the internal communication with the CPU of the plug-in card via an Ethernet connection, you have to include a virtual CP where the IP address may only differ from the IP address of the Ethernet portion of your CPU 51xS plug-in card in the Host-ID.

A CP 343-1 is only available in the hardware catalog if you've installed the Siemens net components. Afterwards the CP is listed under `Simatic300/CP-300/Industrial Ethernet`.

- Add the CP 343-1 (343-1EX11-0XE0) at plug-in location 4
- Click on the CP and enter the according IP address and subnet mask under *Object properties*.

Configure DP master system

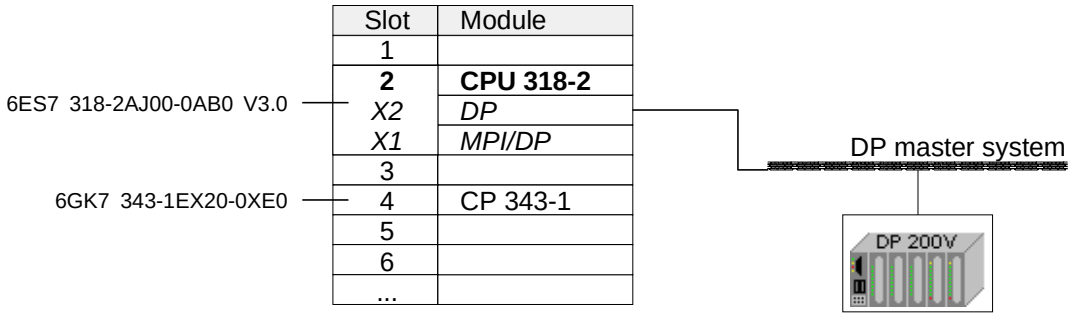
For the project engineering of the DP master system, you have to execute the following steps:

- Right click on *DP* and choose "Add Master System ".
- Create a new Profibus subnet with NEW. This subnet allows you to configure your Profibus slave modules.

Include DP slaves

- For the project engineering of Profibus-DP slaves, choose the according Profibus-DP slave from the *hardware catalog* and move it to the subnet of your master.
- Assign a valid Profibus address to the DP slave.
- Include the modules of the DP slave system in plugged sequence and assign valid addresses to the modules.
- Parameterize the modules if needed.

The following illustration shows the project engineering. Additionally the picture includes a VIPA Profibus-DP slave as example:



Transfer project

By addressing the "Intel" Ethernet interface in your programming res. parameterization tool, you may internally access the CPU and the Profibus master.

The integrated MPI interface allows you to transfer your project from an external programming unit to the plug-in card using the "destination system" functions. At delivery state, the CPU 51xS plug-in card has the MPI address 2.

During start-up, the CPU transfers the Profibus project to the master.

Setting the CPU parameters

Parameters CPU 318-2DP

The parameters of the CPU are set in the hardware configurator from Siemens via the properties of the CPU 318-2DP.

A double-click onto the CPU 318-2DP leads you to the parameterization window of the CPU. The single register tabs show the parameters of the CPU.

Please regard that at this time, not all parameters are supported.

Supported parameters

The CPU doesn't evaluate all parameters that are listed in your project engineering tool. The following parameters are taken into account at this moment:

General :
- MPI address of the CPU
- Baud rate (19.2 kB, 187.5 kB, 1.5 MB)
- max. MPI address

Start-up :
- Start-up when expected/actual configuration differ
- Finished message by modules
- Transfer of parameters to modules

Retentive Memory :
- Number of memory bytes starting with MB0
- Number of S7 timer starting T0
- Number of S7 counters starting with C0

Protection :
- Level of protection/password

Memory :
- Local data
- Bytes of max.

Time-of-Day Interrupts :
- OB10 : Execution, Active
  Start date, time
- OB11 : Execution, Active
  Start date, time

Cyclic Interrupts :
- OB32 : Execution, phase shift
- OB35 : Execution

Cycle/Clock Memory :
- Scan cycle monitoring time
- Minimum scan cycle time
- Scan cycle load from communication
- OB85 - call up at I/O access error
- Clock memory with number

Setting IP address and subnet mask of the CPU

IP address and subnet mask are entered via the properties of the virtually integrated CP 343-1.

Transfer project

Overview

The following options are available to transfer a project into your CPU res. the DP master:

- internal via an Ethernet connection
- external via MPI
- external via MMC memory module

Transfer within project as Ethernet connection

As soon as the PC plug-in card is build in and the according Windows driver file has been installed, the plug-in card is included as Ethernet interface. By addressing the Ethernet interface "Intel(R) 8255xER in your programming res. parameterization tool, you may internal access the CPU and the Profibus master.

As destination IP parameters, the IP parameters of the virtual CP 343-1 are used that you've entered during the project engineering.

If the destination station defined by the IP parameters is not found during the transfer, you may enter the original destination IP parameters for the CPU portion via a dialog window. With the verification of your entries, your project is transferred to the original IP address. After reboot of the CPU, the new IP parameters are active.

Default IP parameters

IP address: 192.168.201.3
Subnet mask: 255.255.255.0

Transfer project external via MPI

If you use an external programming device, you may transfer your data into the CPU 51S via the integrated MP^2I interface. The plug-in card is delivered with the MPI address 2.

If your programming device is not provided with a MPI jack, you may use the "Green Cable" from VIPA to establish a serial point-to-point connection from your PC to MPI. The "Green Cable" has the order no. VIPA 950-0KB00 and may exclusively employed at the according VIPA components.

MPI network

For building up a MPI network, the cables and plugs are similar to those of a 1.5MBaud Profibus network.

Please also regard the chapter "Hints for the employment of the MPI interface"!

The same rules are valid and per default, the MPI network runs at 187kBaud. Every bus participant identifies itself at the bus with an unambiguous MPI address.

Just like Profibus, a core connection must be terminated with its ripple resistor at both ends. Take care that the participants with the activated terminating resistors are always provided with voltage.

Approach

- Connect your PU res. your PC with your CPU via MPI.
- Use **PLC** > *Load to module* in your project engineering tool to transfer the project into the CPU.

Note!

If your programming device is not provided with a MPI jack, you may use the "Green Cable" from VIPA to establish a serial point-to-point connection from your PC to MPI. The "Green Cable" may exclusively employed at the according VIPA components. For the employment of the Green Cable, the MPI interface has to be reconfigured. More detailed information follows on the next pages.

Configure MPI for Green Cable

Information for the configuration of a MPI interface is to find in the documentation of your programming software.

This text describes only the employment of the "Green Cable" from VIPA together with the programming tool from Siemens.

The "Green Cable" establishes a serial connection between the COM interface of the PCs and the MP^{2}I jack of the CPU via MPI.

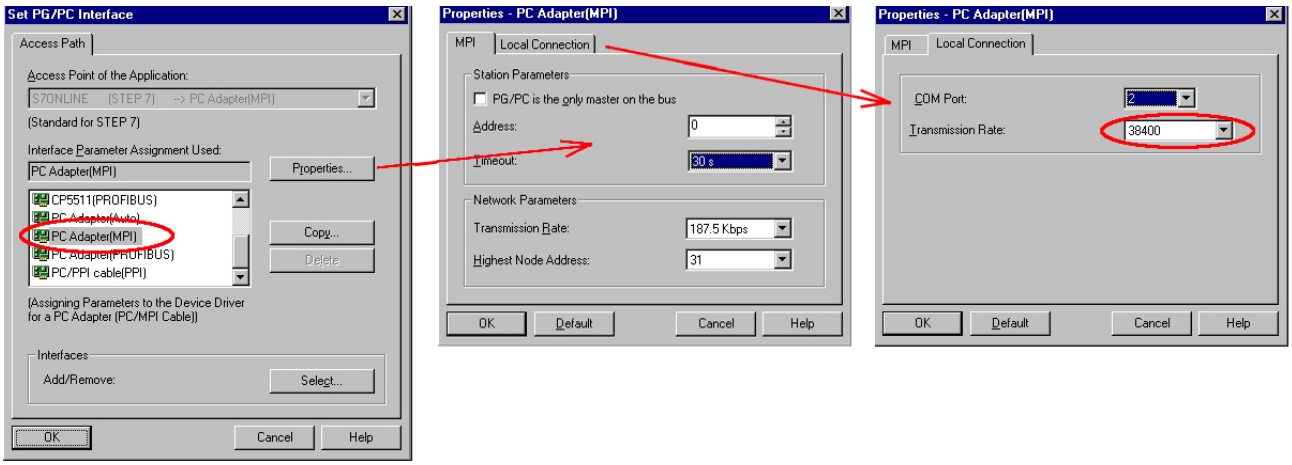
Attention!

Please regard that the "Green Cable" may exclusively be employed immediately at the MP^{2}I jacks of VIPA components!

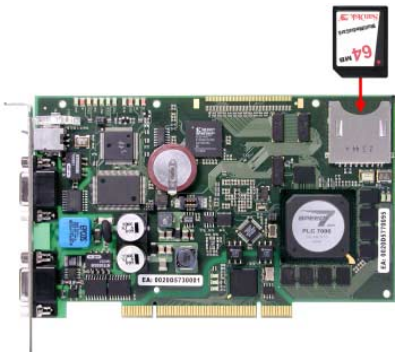
Approach for the MPI configuration

- Open the STEP®7 manager from Siemens and choose **Options** > *Set PU/PC interface*.
- Select "PC Adapter (MPI)" in the option list; if it misses, you first have to add it. Click on [Properties].

  → The following 2 sub dialog boxes allow you to configure your PC adapter to 38400 Baud like shown in the picture:



Employment of the MMC



As external storage medium, the Multi Media Card (MMC) is used (Order no. VIPA 953-0KX10).

A read access of the MMC is always executed after an OVERALL_RESET.

To write onto the MMC you either use a write command from the hardware configurator from Siemens or a MMC reading device from VIPA (Order no. VIPA 950-0AD00). This allows you to program applications at the PC, to copy them to the MMC and to easily transfer them to the VIPA CPU. The MMC modules are delivered from VIPA pre-formatted with the FAT16 file system.

There may be stored several projects and subdirectories on a MMC memory module.

Please take care that your recent project engineering is stored at the root directory and has the file name: **S7PROG.WLD.**

Transfer CPU → MMC

When a MMC is plugged in the CPU, a write command transfers the content of the battery buffered RAM to the MMC.

Initialize the write command via the hardware configurator from Siemens by selecting **PLC** > *Copy RAM to ROM*.

During the write process, the yellow "MMC"-LED of the CPU is blinking.

Simultaneously, a write process into the internal flash of the CPU is executed.

Control the transfer process via event-IDs

After a write process at the MMC, an according ID-event is entered into the diagnostic buffer of the CPU. To monitor the diagnostic entries, choose **PLC** > *Module status* in your STEP®7 manager. The register "Diagnostic buffer" leady you to the diagnosis window.

Writing onto the MMC can cause the following events:

Event-ID	Description
0xE100	MMC access error
0xE101	MMC error file system
0xE102	MMC error FAT
0xE200	Write to MMC ready
0xE300	Write internal flash ready

Note!

If the size of the user application exceeds the user memory of the CPU, the content of the MMC is not transferred.

It is considered to compress the user application before the transfer. This is not automatically executed.

Transfer MMC → CPU after overall reset

The transfer of the user application from the MMC to the CPU is always executed after an OVERALL_RESET. The transfer process is indicated by the blinking of the yellow LED "MMC" at the CPU.

If there is no valid user application at the MMC or if the transfer fails, an OVERALL_RESET of the CPU is executed and the STOP-LED blinks three times.

Operating modes of the CPU 51xS

Overview

The CPU has 4 operating modes:

- operating mode STOP
- operating mode START-UP
- operating mode RUN
- operating mode FLAG

Certain conditions in the operating modes START-UP and RUN require a specific reaction from the system program. In this case the application interface is often provided by a call to an organization block that was included specifically for this event.

Operating mode STOP

- Processing of the application program has stopped.
- If the program was being processed before, the values of counters, timers, flags and the contents of the process image are retained during the transition to the STOP mode.
- Outputs are inhibited, i.e. all digital outputs are disabled.
- RUN-LED off
- STOP-LED on

Operating mode START-UP

- During the transition from STOP to RUN a call is issued to the start-up organization block OB 100. The length of this OB is not limited. The processing time for this OB is not monitored. The start-up OB may issue calls to other blocks.
- All digital outputs are disabled during the start-up, i.e. outputs are inhibited.
- RUN-LED blinks
- STOP-LED off

When the CPU has completed the start-up OB, it assumes the operating mode RUN.

Operating mode RUN

- The application program in OB 1 is processed in a cycle. Under the control of alarms other program sections can be included in the cycle.
- All timers and counters, being started by the program, are active and the process image is updated with every cycle.
- The BASP-signal (outputs inhibited) is deactivated, i.e. all digital outputs are enabled.
- RUN-LED on
- STOP-LED off

Operating mode FLAG

The CPU 51xS provides the opportunity to define up to 4 break points (flags) for program diagnosis purposes. The flags are set and deleted via your programming neighborhood. As soon as a break point is reached, you may execute your application line by line and may activate in- and outputs.

Preconditions

For the usage of break points, the following preconditions must be fulfilled:

- The single step test mode is only available for STL, if needed, change the view via **View** > *STL* to STL.
- The block has to be opened online and must not be protected.
- The opened block must not have been altered in the editor.

Approach with break points

- Activate the break point bar via **View** > *Break point bar*.
- Put the cursor to the statement line where a break point is to be set.
- Set the break point with **Test** > *Set break point*. The statement line is marked with a ring.
- To activate the break point, choose **Test** > *Break point active*. The ring changes to a circle.
- Switch the CPU to RUN. When the user application reaches the break point, the CPU switches into the state FLAG, the break point is marked with an arrow and the register contents are shown.
- Now you may execute your application code step by step via **Test** > *Next command* or execute the application until the next break point with **Test** > *Continue*.
- **Test** > *Delete (all) break points* deletes (all) break points.

Behavior in operating mode FLAG

- LED RUN blinks and LED STOP is on.
- The code execution has been stopped. All run levels are not executed.
- All timer are frozen.
- The real-time clock is still active.
- The outputs are shut down, but may be released for test purposes.
- Passive CP communication is possible.

Note!

The usage of break points is possible at any time. A switch to the operating mode “Test operation” is not required.

If you set more than 3 break points, the single step operation is not longer available.

Function security

The CPUs include security mechanisms like a Watchdog (100ms) and a parameterizable cycle time surveillance (parameterizable min. 1ms) that stop res. execute a RESET at the CPU in case of an error and set it into a defined STOP state.

The VIPA CPUs are developed function secure and have the following system properties:

Event	concerns	Effect
RUN → STOP	general	BASP (**B**efehls-**A**usgabe-**Sp**erre, i.e. command output lock) is set.
	central digital outputs	The outputs are set to 0V.
	central analog outputs	The voltage supply for the output channels is switched off.
	decentral outputs	The outputs are set to 0V.
	decentral inputs	The inputs are read constantly from the slave and the recent values are put at disposal.
STOP → RUN res. Power on	general	First the PII is deleted, the call of the OB100 follows. After the execution of the OB, the BASP is set back and the cycle starts with: Delete PIO → Read PII → OB1.
	central analog outputs	The behavior of the outputs at restart can be preset.
	decentral inputs	The inputs are read constantly from the slave and the recent values are put at disposal.
RUN	general	The program execution happens cyclically and can therefore be foreseen: Read PII → OB1 → Write PIO.

PII: = Process image inputs

PIO: = Process image outputs

DP master operating modes

STOP → RUN (automatically)

After NETZ_EIN (i.e. POWER_ON) and with valid project engineering data, the DP master switches automatically to RUN. We abstained an operating mode lever for the DP master.

After a POWER ON automatically the project engineering data and bus parameters are send from the CPU to the DP master. This establishes a communication to the DP slaves. At successful connection and valid bus parameters, the DP master switches to Data Exchange (DE). The LEDs RUN and DE are on.

When receiving wrong/invalid parameters, the DP master switches to RUN and monitors a parameterization error via the IF-LED.

The DP master is now linked up to the bus with the following default bus parameters:

Default-Bus-Parameter: Address: 1; Transfer rate: 1.5 MBaud.

RUN

During RUN mode, the RUN- and the DE-LEDs are on. Now data may be transferred. In the event of an error, like e.g. a DP slave break down, this is shown at the DP master via the ERR-LED and an alarm to the CPU is initiated.

Note!

If the CPU switches to STOP during operation, the DP master stays in RUN. Due to the BASP signal, all outputs of the peripheral modules connected via DP slaves are set to zero.

After a slave failure, the process image of the inputs keeps the status of before the slave failure.

Overall_Reset

Outline

During the OVERALL_RESET the entire user memory (RAM) and the remanent memory area is erased.

Data located in the memory card is not affected.

You should always issue an overall reset to your CPU before loading an application program into your CPU, to ensure that all blocks have been cleared from it.

OVERALL_RESET by means of the function selector

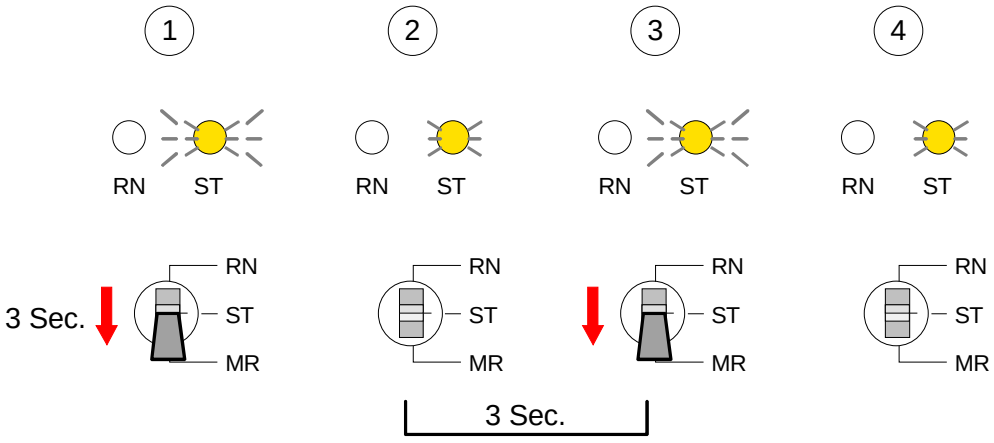
Condition

The operating mode of the CPU is STOP. Place the function selector on the CPU in position "STOP" → The ST-LED is on.

OVERALL_RESET

- Place the function selector in the position MR and hold it in this position for app. 3 seconds. → The ST-LED changes from blinking to permanently on.
- Place the function selector in the position STOP and switch it to MR and quickly back to STOP within a period of less than 3 seconds.
  → The ST-LED blinks (overall reset procedure).
- The overall_reset has been completed when the STOP-LED is on permanently. → The ST-LED is on.

The following figure illustrates the above procedure:



Overall_reset via PLC-Tool

At deployment of the operating software PLC-Tool you may initialize the OVERALL_RESET via the button [M-RES].

The button is available as soon as your CPU is in STOP.

OVERALL_RESET via STEP®7 Manager from Siemens

Conditions

Your CPU has to be in STOP.
Via the menu command **PLC** > *Operating Mode* you switch your CPU in STOP.

OVERALL_RESET

Via the menu command **PLC** > *Clear/Reset* you request the OVERALL_RESET.

In the dialog window you may switch your CPU to STOP if you didn't that yet and start the OVERALL_RESET.

During the OVERALL_RESET procedure the STOP-LED is blinking.

When the STOP-LED changes to permanently on, the OVERALL_RESET has been finished.

Automatic reload

After the OVERALL_RESET the CPU attempts to reload the parameters and the program from the memory card. → The MMC-LED blinks.

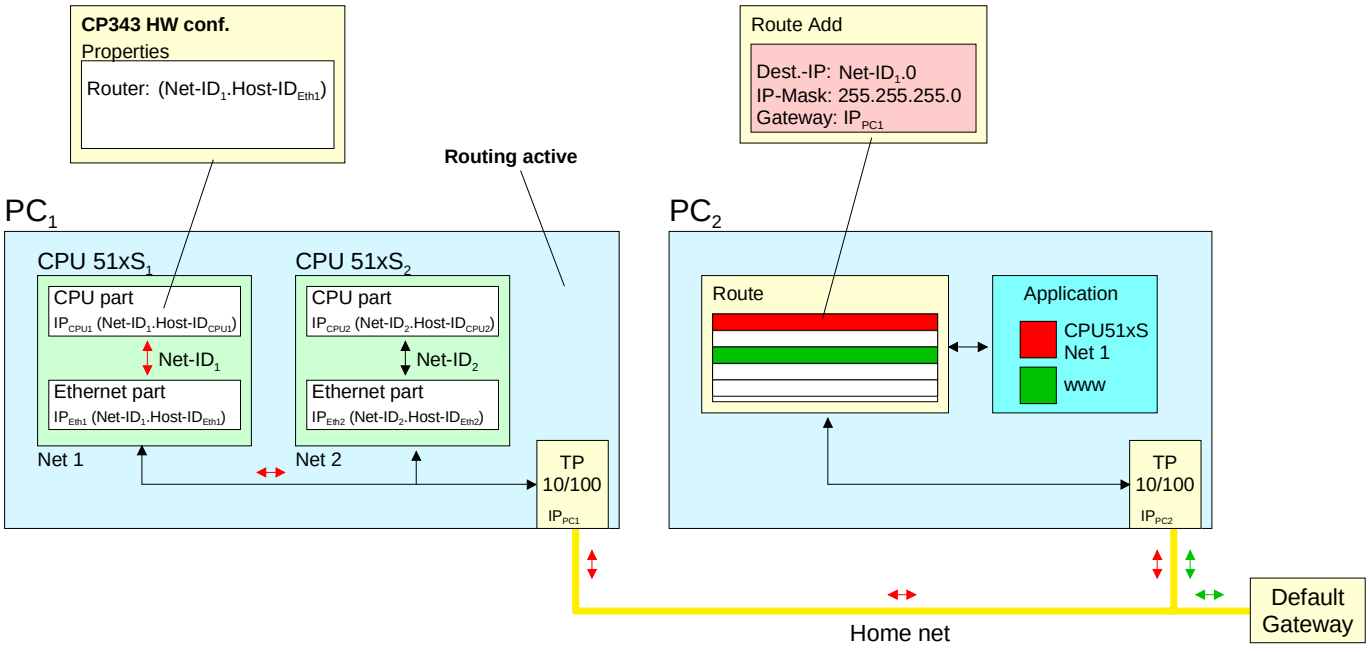
When the reload has been completed, the LED extinguishes. The operating mode of the CPU will be STOP or RUN, depending on the position of the function selector.

Confirm external access via Ethernet

Overview

You may access the CPU 51xS from an external PC via Ethernet. The following preconditions must be fulfilled:

- The routing is activated on the PC with the CPU 51xS
- The route is entered at the CPU 51xS via a CP343 hardware configuration with the following parameters:
  - Destination router: IP address of the Ethernet component IP_{Eth} of the CPU 51xS
- The route is entered at the external PC with the following parameters:
  - Destination-IP: Net-ID of the Ethernet component of the CPU 51xS
  - IP-Mask: subnet mask of the CPU 51xS (default: 255.255.255.0)
  - Gateway: IP address of the PCs IP_{PC} with the CPU 51xS at the home network



Attention!

Only a trained system administrator should execute changes at the network neighborhood for this may cause conflicts with the company network!

The employment under Windows 9x res. Windows XP Home is not recommended and not described.

Activate routing

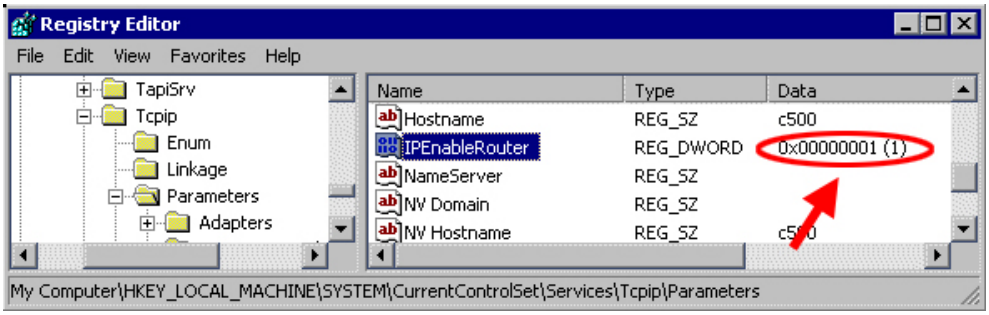
The following text describes the steps of configuration. More detailed information especially to the operating system specific routing is to find in the documentation of the operating system.

Activation under Windows NT4 / 2000$_{Server}$ / 2003$_{Server}$

The activation of the routing happens in the "Network neighborhood properties" at the properties of the TCP/IP protocol.

Activation under Windows XP$_{Professional}$ / 2000$_{Professional}$

For the activation, an entry into the registry file is required like illustrated below:



After a reboot, the routing is active.

Enter route

The entry of a route happens exclusively via the command console of the operating system by using the "route" command. The following parameters are required:

route ADD <Destination-IP> MASK <IP-Mask> <Gateway> METRIC <Metric> IF <IF>

with

ADD: Command for adding a route

Dest.-IP: IP address of the network (Net-ID) of the CPU 51xS

IP-Mask: Subnet mask of the net of the CPU 51xS

Gateway: IP address of the destination computer at the home network with the plugged CPU 51xS

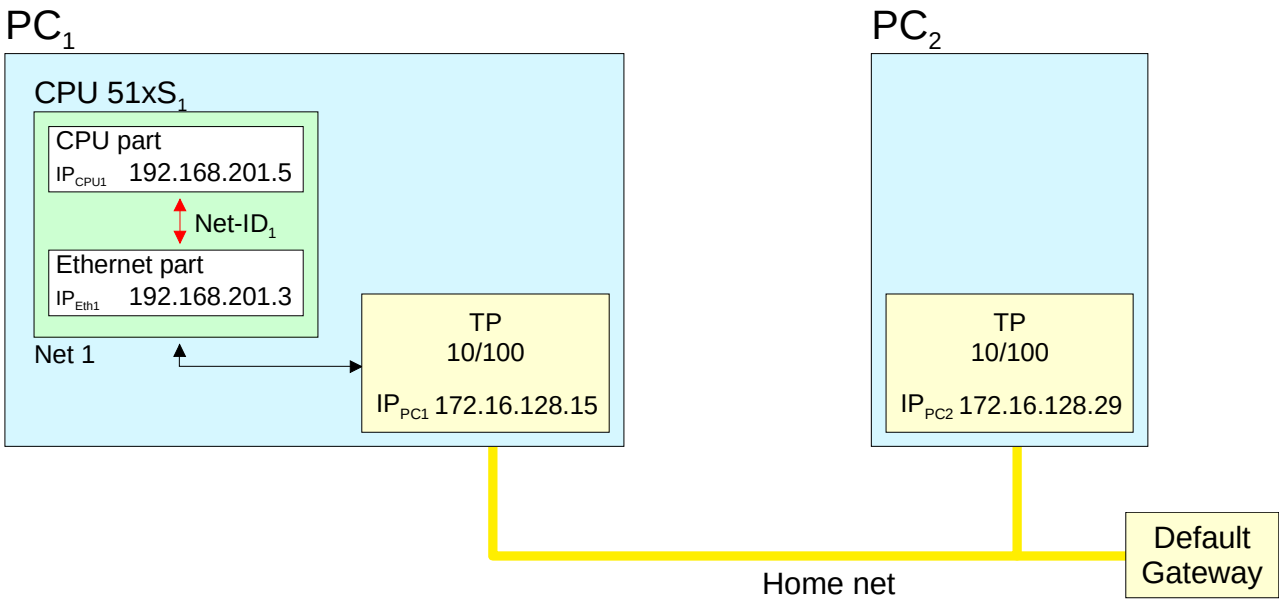
Metric: (optional) Price value for a destination

IF: (optional) Preset interface or best alternate interface

route PRINT lists all entered routes

route DELETE <Destination-IP> deletes the entry

Example: The following constellation is present and you want to access the CPU via PC:



- Activate the routing at PC1 like described above.
- Start the hardware configurator from Siemens and configure a system with CP 343.
- Enter the IP address 192.168.201.5 and the subnet mask 255.255.255.0 in "Properties Ethernet interface".
- Choose the function “Use router” under "Parameter", enter the IP address 192.168.201.3 of the Ethernet portion of the CPU 51xS as "Gateway" and transfer your project.
- Start the command console at PC2 and enter the following statement:

  ```
  route add 192.168.201.0 mask 255.255.255.0 172.16.128.15
  ```

Now you may access the CPU from PC2 via PC1. You may test the connection with the command `ping 192.168.201.5`.

Control and monitoring of variables

Outline

For troubleshooting purposes and to display the status of certain variables you can access certain test functions via the menu item **Test** of the Siemens STEP®7 Manager.

The status of the operands and the VKE can be displayed by means of the test function **Debug** > *Monitor*.

You can modify and/or display the status of variables by means of the test function **PLC** > *Monitor/Modify Variables*.

Debug > *Monitor*

This test function displays the current status and the VKE of the different operands while the program is being executed.

It is also possible to enter corrections to the program.

Note!

When using the test function “Monitor” the PLC must be in RUN mode!

The processing of statuses can be interrupted by means of jump commands or by timer and process-related alarms. At the breakpoint the CPU stops collecting data for the status display and instead of the required data it only provides the PG with data containing the value 0.

For this reason, jumps or time and process alarms can result in the value displayed during program execution remaining at 0 for the items below:

- the result of the logical operation VKE
- Status / AKKU 1
- AKKU 2
- Condition byte
- absolute memory address SAZ. In this case SAZ is followed by a "?".

The interruption of the processing of statuses does not change the execution of the program. It only shows that the data displayed is no longer valid from the point on, where the interrupt occurred.

PLC >
Monitor/Modify Variables

This test function returns the condition of a selected operand (inputs, outputs, flags, data word, counters or timers) at the end of program-execution.

This information is obtained from the process image of the selected operands. During the "processing check" or in operating mode STOP the periphery is read directly from the inputs. Otherwise only the process image of the selected operands is displayed.

Control of outputs

It is possible to check the wiring and proper operation of output-modules.

You can set outputs to any desired status with or without a control program. The process image is not modified but outputs are no longer inhibited.

Control of variables

The following variables may be modified:

E, A, M, T, Z and D.

The process image of binary and digital operands is modified independently of the operating mode of the CPU 31x.

When the operating mode is RUN the program is executed with the modified process variable. When the program continues they may, however, be modified again without notification.

Process variables are controlled asynchronously to the execution sequence of the program.

Integrated OBs, SFCs, SFBs

The following organization blocks (OBs) are available:

OB	Description
OB 1	Free cycle
OB 10	Clock alarm
OB 11	Clock alarm
OB 20	Delay alarm
OB 21	Delay alarm
OB 32	Prompter alarm
OB 35	Prompter alarm
OB 40	Process alarm
OB 41	Process alarm
OB 80	Cycle time exceeded or clock alarm run out
OB 82	Diagnostic alarm
OB 85	OB not available
OB 86	Slave failure res. restart
OB 100	Reboot
OB 121	Synchronous errors
OB 122	Periphery error at n^{th} access

The following system function blocks (SFBs) are available:

SFB	Label	Description
SFB 0	CTU	Count up
SFB 1	CTD	Count down
SFB 2	CTUD	Count up and down
SFB 3	TP	Create pulse
SFB 4	TON	Create turn-on delay
SFB 5	TOF	Create turn-off delay
SFB 32	DRUM	realize a step-by-step switch with maximum 16 steps

The following standard system functions (SFCs) are available:

SFC	Label	Description
SFC 0	SET_CLK	Set clock
SFC 1	READ_CLK	Read clock
SFC 2	SET_RTM	Set operating time counter
SFC 3	CTRL_RTM	Start/stop operating time counter
SFC 4	READ_RTM	Read operating time counter
SFC 5	GADR_LGC	Get logical address of a channel (only for modules at rack 0)
SFC 6	RD_SINFO	Read start information of the recent OB
SFC 12	D_ACT_DP	Activation or deactivation of DP slaves
SFC 13	DPNRM_DG	Read slave diagnostic data
SFC 14	DPRD_DAT	Read consistent user data (also from DP slaves → DP master FW ≥ V3.00)
SFC 15	DPWR_DAT	Write consistent user data (also to DP slaves → DP master FW ≥ V3.00)
SFC 20	BLKMOV	Copy variable inside work memory
SFC 21	FILL	Predefine field inside work memory
SFC 22	CREAT_DB	Create data block
SFC 23	DEL_DB	Delete data block
SFC 24	TEST_DB	Test data block
SFC 28	SET_TINT	Set clock alarm
SFC 29	CAN_TINT	Cancel clock alarm
SFC 30	ACT_TINT	Activate clock alarm
SFC 31	QRY_TINT	Request clock alarm
SFC 32	SRT_DINT	Start delay alarm
SFC 33	CAN_DINT	Cancel delay alarm
SFC 34	QRY_DINT	Request delay alarm
SFC 36	MASK_FLT	Mask synchronous error events
SFC 37	DMASK_FLT	Demask synchronous error events
SFC 38	READ_ERR	Read event status register
SFC 41	DIS_AIRT	Delay alarm events
SFC 42	EN_AIRT	Cancel alarm event delay
SFC 43	RE_TRIGR	Re-trigger cycle time surveillance
SFC 44	REPL_VAL	Transfer replacement value into ACCU1
SFC 46	STP	Switch CPU in STOP
SFC 47	WAIT	Delay program processing additionally to delay time
SFC 49	LGC_GADR	Search the plug-in location concerning to a logical address
SFC 50	RD_LGADR	Search all logical addresses of a block
SFC 51	RDSYSST	Read information from system state list
SFC 52	WR_USMSG	Write user entry into diagnostic buffer (sending via MPI in preparation)
SFC 54	RD_DPARM	Read predefined parameters
SFC 55	WR_PARM	Write dynamic parameters (only for analog, digital blocks, FM350, CP340 / not possible via Profibus)

continue ...

... continue

SFC 56	WR_DPARM	Write predefined parameters (only for analog, digital blocks, FM350, CP340 / not possible via Profibus)
SFC 57	PARM_MOD	Parameterize block (only for analog, digital blocks, FM350, CP340 / not possible via Profibus)
SFC 58	WR_REC	Write record set (only for analog, digital blocks, FM350, CP340 / not possible via Profibus)
SFC 59	RD_REC	Read record set (only for analog, digital blocks, FM350, CP340 / not possible via Profibus)
SFC 64	TIME_TICK	Read millisecond timer
SFC 65	X_SEND	Send data to external partner
SFC 66	X_RCV	Receive data from external partner
SFC 67	X_GET	Read data from external partner
SFC 68	X_PUT	Write data to external partner
SFC 69	X_ABORT	Interrupt connection to external partner
SFC 81	UBLKMOV	Copy variable uninterruptible

The following VIPA specific SFCs are available:

SFC	Label	Description
SFC 208	FILE_OPN	Open VIPA file
SFC 209	FILE_CRE	Create VIPA file
SFC 210	FILE_CLO	Close VIPA file
SFC 211	FILE_RD	Read VIPA file
SFC 212	FILE_WR	Write VIPA file
SFC 213	FILE_SEK	Seek VIPA file
SFC 214	FILE_REN	Rename VIPA file
SFC 215	FILE_DEL	Delete VIPA file
SFC 219	CAN_TLGR	Send VIPA CAN telegram
SFC 227	TD_PRM	VIPA parameterization for TD200 communication
SFC 228	RW_Kachel	Read/write VIPA page frame
SFC 230	Send	VIPA handling block for page frame communication
SFC 231	Receive	VIPA handling block for page frame communication
SFC 232	Fetch	VIPA handling block for page frame communication
SFC 233	Control	VIPA handling block for page frame communication
SFC 234	Reset	VIPA handling block for page frame communication
SFC 235	Synchron	VIPA handling block for page frame communication
SFC 236	Send_All	VIPA handling block for page frame communication
SFC 237	Recv_All	VIPA handling block for page frame communication
SFC 238	Control1	VIPA handling block for page frame communication

Technical Data

Electrical Data	VIPA 517-2AJ00
Supply voltage (external)	DC 24V (-15% ... +20%)
Current consumption	max. 1 A
Dissipation power	5 W
System Data	
Program memory internal	1MByte
Load memory	1MByte
Memory external	MMC
Accu buffer/Clock	yes/yes
Bit memory	8192
Timer/Counter	256/256
Addressable I/O	
- digital	1024
- analog	128
Processing time Bit/Word	typ. 0.18ms / 0.78ms/k
Modules	OB1/10/35/40/100
- FBs	1024
- FCs	1024
- DBs	2047
Interfaces	
- MP^2I	8 static and 8 dynamic MPI connections / 187 kBaud, RS232: 38,4kBaud
- DP master	9.6kBaud to 12MBaud
Operating conditions	
Operating temperature	0°C...+60°C
Storing temperature	-25°C...+70°C
Relative humidity	95% without condensation
EMV/BURST/ESD	EN 61000-4-2 / EN 61000-4-4 (up to Level 3: 8kV / 2,5kV)
Supplements	
WinPLC7 Programming tool	VIPA WinPLC7
MMC storage module	VIPA 953-0KX00
USB-MMC reading device	VIPA 950-0AD00
Green Cable	VIPA 950-0KB00
Measurements	
Length x Width	174 x 106 (1 PCI-Slot)

Appendix

A Index

M.Stich